DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE MATERIALS

ECT 301:LINEAR INTEGRATED CIRCUITS

VISION OF THE INSTITUTION

To mould true citizens who are millennium leaders and catalysts of change through excellence in education.

MISSION OF THE INSTITUTION

NCERC is committed to transform itself into a center of excellence in Learning and Research in Engineering and Frontier Technology and to impart quality education to mould technically competent citizens with moral integrity, social commitment and ethical values.

We intend to facilitate our students to assimilate the latest technological know-how and to imbibe discipline, culture and spiritually, and to mould them in to technological giants, dedicated research scientists and intellectual leaders of the country who can spread the beams of light and happiness among the poor and the underprivileged.

ABOUT DEPARTMENT

- Established in: 2002
- Course offered : B.Tech in Electronics and Communication Engineering

  M.Tech in VLSI
- Approved by AICTE New Delhi and Accredited by NAAC
- Affiliated to the University of Dr. A P J Abdul Kalam Technological University.

DEPARTMENT VISION

Providing Universal Communicative Electronics Engineers with corporate and social relevance towards sustainable developments through quality education.

DEPARTMENT MISSION

1) Imparting Quality education by providing excellent teaching, learning environment.

2) Transforming and adopting students in this knowledgeable era, where the electronic gadgets (things) are getting obsolete in short span.

3) To initiate multi-disciplinary activities to students at earliest and apply in their respective fields of interest later.

4) Promoting leading edge Research & Development through collaboration with academia & industry.

PROGRAMME EDUCATIONAL OBJECTIVES

PEOI. To prepare students to excel in postgraduate programmes or to succeed in industry / technical profession through global, rigorous education and prepare the students to practice and innovate recent fields in the specified program/ industry environment.

PEO2. To provide students with a solid foundation in mathematical, Scientific and engineering fundamentals required to solve engineering problems and to have strong practical knowledge required to design and test the system.

PEO3. To train students with good scientific and engineering breadth so as to comprehend, analyze, design, and create novel products and solutions for the real life problems.

PEO4. To provide student with an academic environment aware of excellence, effective communication skills, leadership, multidisciplinary approach, written ethical codes and the life-long learning needed for a successful professional career.

PROGRAM OUTCOMES (POS)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSO)

PSO1: Ability to Formulate and Simulate Innovative Ideas to provide software solutions for Real-time Problems and to investigate for its future scope.

PSO2: Ability to learn and apply various methodologies for facilitating development of high quality System Software Tools and Efficient Web Design Models with a focus on performance

optimization.

PSO3: Ability to inculcate the Knowledge for developing Codes and integrating hardware/software products in the domains of Big Data Analytics, Web Applications and Mobile Apps to create innovative career path and for the socially relevant issues.

COURSE OUTCOMES
ECT 301

SUBJECT CODE: EC 308	
COURSE OUTCOMES	
C301.1	Learn about the basic concepts for the circuit configuration for the design of linear integrated circuits and develops skill to solve engineering problems.
C301.2	Develop skills to design simple circuits using OP-AMP.
C301.3	Gain knowledge about oscillators and multivibrators.
C301.4	Gain knowledge about PLL.
C301.5	Learn about various techniques to develop A/D and D/A convertors.

MAPPING OF COURSE OUTCOMES WITH PROGRAM OUTCOMES

CO'S	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
C301.1	2	1	3	2		3						
C301.2	1	2	2	1	2	2		2				
C301.3	3	2	2	1	2	1					2	1
C301.4	2	2	2	2								1
C301.5	3	3	3	2	2							1
C301	3	2	2	2	2	1	2	2			2	1

CO'S	PSO1	PSO2	PSO3
C301.1	2	2	
C301.2	2		
C301.3	3		
C301.4	3		2
C301.5	3	3	2
C301	3	2	1

SYLLABUS

ECT301	LINEAR INTEGRATED CIRCUITS	CATEGORY	L	T	P	CREDITS
		PCC	3	1	0	4

Preamble: This course aims to develop the skill to design circuits using operational amplifiers and other linear ICs for various applications.

Prerequisite: EC202 Analog Circuits

Course Outcomes: After the completion of the course the student will be able to

CO 1	Understand Op Amp fundamentals and differential amplifier configurations
CO 2	Design operational amplifier circuits for various applications
CO 3	Design Oscillators and active filters using opamps
CO4	Explain the working and applications of timer, VCO and PLL ICs
CO5	Outline the working of Voltage regulator IC's and Data converters

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12
CO 1	3	3	1	2								1
CO 2	3	3	2	2	2							1
CO 3	3	3	2	2	2							1
CO 4	3	3	1	2	2							1
CO 5	3	3	2	2	2							1

Assessment Pattern

Bloom's Category		Continuous Assessment Tests		End Semester Examination
		1	2	
Remember	K1	10	10	10
Understand	K2	30	30	60
Apply	K3	10	10	30
Analyse	K4			
Evaluate				
Create				

Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	50	100	3 hours

SYLLABUS

Module 1:

Operational amplifiers(Op Amps): The 741 Op Amp, Block diagram, Ideal op-amp parameters, typical parameter values for 741, Equivalent circuit, Open loop configurations, Voltage transfer curve, Frequency response curve.

Differential Amplifiers: Differential amplifier configurations using BJT, DC Analysis- transfer characteristics; AC analysis- differential and common mode gains, CMRR, input and output resistance, Voltage gain. Constant current bias, constant current source; Concept of current mirror-the two transistor current mirror, Wilson and Widlar current mirrors.

Module 2:

Op-amp with negative feedback: General concept of Voltage Series, Voltage Shunt, current series and current shunt negative feedback, Op Amp circuits with voltage series and voltage shunt feedback, Virtual ground Concept; analysis of practical inverting and non-inverting amplifiers for closed loop gain, Input Resistance and Output Resistance.
Op-amp applications: Summer, Voltage Follower-loading effects, Differential and Instrumentation Amplifiers, Voltage to current and Current to voltage converters, Integrator, Differentiator, Precision rectifiers, Comparators, Schmitt Triggers, Log and antilogamplifiers.

Module 3:

Op-amp Oscillators and Multivibrators: Phase Shift and Wien-bridge Oscillators, Triangular and Sawtooth waveform generators, Astable and monostable multivibrators.
Active filters: Comparison with passive filters, First and second order low pass, High pass, Band pass and band reject active filters, state variable filters.

Module 4 :

Timer and VCO: Timer IC 555- Functional diagram, Astable and monostable operations;. Basic concepts of Voltage Controlled Oscillator and application of VCO IC LM566,
Phase Locked Loop – Operation, Closed loop analysis, Lock and capture range, Basic building blocks, PLL IC 565, Applications of PLL.

Module 5:

Voltage Regulators: Fixed and Adjustable voltage regulators, IC 723 – Low voltage and high voltage configurations, Current boosting, Current limiting, Short circuit and Fold-back protection.
Data Converters: Digital to Analog converters, Specifications, Weighted resistor type and R-2R Ladder type.
Analog to Digital Converters: Specifications, Flash type and Successive approximation type.

Text Books

1. Roy D. C. and S. B. Jain, Linear Integrated Circuits, New Age International, 3/e, 2010

Reference Books

1. DFranco S., Design with Operational Amplifiers and Analog Integrated Circuits, 3/e, Tata McGraw Hill, 2008
2. Gayakwad R. A., Op-Amps and Linear Integrated Circuits, Prentice Hall, 4/e, 2010
3. Salivahanan S. and V. S. K. Bhaaskaran, Linear Integrated Circuits, Tata McGraw Hill, 2008.
4. Botkar K. R., Integrated Circuits, 10/e, Khanna Publishers, 2010
5. C.G. Clayton, Operational Amplifiers, Butterworth & Company Publ. Ltd. Elsevier, 1971
6. David A. Bell, Operational Amplifiers & Linear ICs, Oxford University Press, 2nd edition, 2010
7. R.F. Coughlin & Fredrick Driscoll, Operational Amplifiers & Linear Integrated Circuits, 6th Edition, PHI, 2001
8. Sedra A. S. and K. C. Smith, Microelectronic Circuits, 6/e, Oxford University Press, 2013.

QUESTION BANK

MODULE I				
Q:NO:	**QUESTIONS**	**CO**	**KL**	**PAGE NO:**
1	Compare CMRR and Slew rate of an op-amp.	CO1	K4	4
2	Sketch the neat diagram and explain the closed loop differential amplifier.	CO1	K3	5
3	Generate the expressions for gain, input impedance, output impedance and frequency response of a voltage series feedback circuit.	CO1	K5	6
4	Sketch the block diagram of an op-amp and explain its necessity and implementation of each block.	CO1	K3	7
5	Compare PSRR and Slew rate of an op-amp.	CO1	K4	8
6	Sketch the neat diagram and explain the closed loop inverting amplifier.	CO1	K3	9
7	Generate the expressions for gain, input impedance, output impedance and frequency response of a voltage shunt feedback circuit.	CO1	K5	9
8	Sketch the block diagram of an op-amp and explain its necessity and implementation of each block.	CO1	K3	9
9	Define the following: a. CMRR b. Slew rate	CO1	K1	10
10	Sketch the neat diagram and explain the closed loop inverting amplifier.	CO1	K3	10
MODULE II				
1	Explain voltage to current converter with a neat diagram.	CO2	K5	11
2	Sketch the suitable diagram and equation; explain how the average of signals can be achieved by using an op-amp.	CO2	K3	12
3	Explain the working of a practical differentiator	CO2	K5	13

	circuit with the circuit diagram.			
4	Design a Schmitt trigger circuit for different UTP and LTP magnitudes.	CO2	K5	15
5	Explain current to voltage converter with a neat diagram.	CO2	K5	16
6	Sketch the suitable diagram and equation; explain how the summing of signals can be achieved by using an op-amp.	CO2	K3	18
7	Explain the working of a practical integrator circuit with the circuit diagram.	CO2	K5	20
8	Design a zero crossing detector and explain its working.	CO2	K5	21
9	Design a circuit to obtain an output of – $(V_1+2V_2+5V_3)$	CO2	K5	22
10	Sketch the suitable diagram and equation; explain how the summing of signals can be achieved by using an op-amp.	CO2	K3	23
	MODULE III			
1	Sketch the neat diagram and derive the frequency of oscillation for RC phase shift oscillator.	CO3	K3	25
2	Sketch the neat diagram and derive the frequency of oscillation for wien-bridge oscillator.	CO3	K3	26
3	Design a second order Butterworth low-pass filter with a upper cutoff frequency 1KHz.	CO3	K5	28
4	Explain the working of a triangular wave form generator with a neat circuit diagram; Also derive an expression for frequency of oscillation.	CO3	K5	30
5	Design a second order Butterworth low-pass filter with a upper cutoff frequency 2KHz.	CO3	K2	31
6	Sketch the first order active low pass filter and derive its transfer function.	CO3	K3	32
7	Explain the working of a square wave form generator with a neat circuit diagram; Also derive an expression for frequency of oscillation of sawtooth wave generator.	CO3	K2	33

	MODULE IV			
1	Discuss in detail any two applications of PLL.	CO4	K4	35
2	Sketch the block diagram of IC 566 VCO and explain its operation.	CO4	K3	36
3	Explain how a monostable multivibrator can be implemented with 555 IC with relevant waveforms and functional diagram. Derive a expression for pulse width.	CO4	K5	37
4	Illustrate the principle of operation of PLL with its capture range and lock range.	CO4	K2	38
5	Discuss in detail any two applications of 555.	CO4	K2	39
6	Sketch the block diagram of IC 565 PLL and explain its operation.	CO4	K3	39
7	Explain how a astable multivibrator can be implemented with 555 IC with relevant waveforms and functional diagram. Derive a expression for pulse width.	CO4	K3	40
8	Illustrate the principle of operation of VCO with its capture range and lock range.	CO4	K5	41
	MODULE V			
1	Discuss the specifications of ADC and DAC.	CO5	K2	42
2	Explain the principle of operation of successive approximation type ADC.	CO5	K5	43
3	Sketch the neat diagram and explain the working of a weighted resistor ADC. Discuss how digital signal is converted into analog signal in a weighted resistor DAC.	CO5	K3	44
4	Compare ADC and DAC.	CO5	K4	45
5	Explain the principle of operation of flash type ADC.	CO5	K5	46
6	Sketch the neat diagram and explain the working of a R-2R resistor DAC. Discuss how digital signal is converted into analog signal in a weighted	CO5	K3	47

	resistor DAC.			

APPENDIX 1		
CONTENT BEYOND THE SYLLABUS		
S:NO;	**TOPIC**	**PAGE NO:**
1	ADC AND DAC	50

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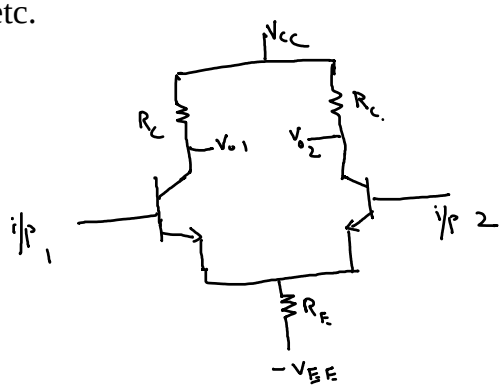
Operational amplifier

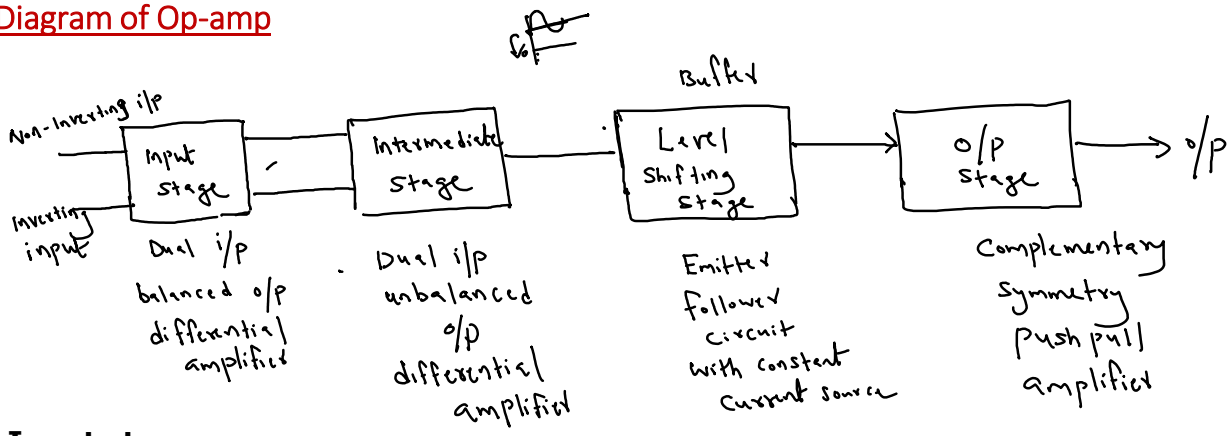
Op-amp

An operational amplifier is a high gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and an output stage.
The output stage is generally a push-pull or push-pull complementary stage.

Op-amp is used to amplify ac and dc signals.
It can perform mathematical operations such as addition, subtraction, multiplication, integration etc.
With addition of some feedback components, op-amp can be operated for ac and dc amplification, active filters, oscillators, comparators, regulators etc.



Block Diagram of Op-amp

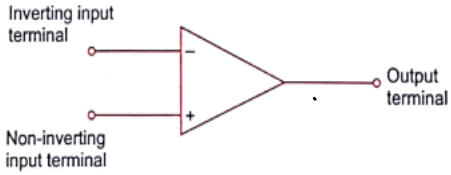


Input stage :
The input stage is a dual-input, balanced output differential amplifier. The two input are inverting and non-inverting input terminals. This stage provides most of the voltage gain of the OP-AMP and decides the input resistance value Ri.

Intermediate stage :
This is usually another differential amplifier. It is driven by the output of the input stage. This stage is a dual-input unbalanced output (single ended output) differential amplifier.

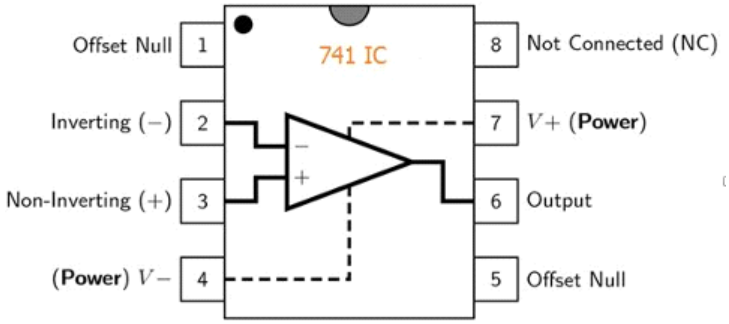
Level shifting stage :
Due to the direct coupling between the first two stages, the input of level of shifting stage is an amplified signal with some non-zero dc level. Level shifting stage is used to bring this dc level to zero volts with respect to ground.

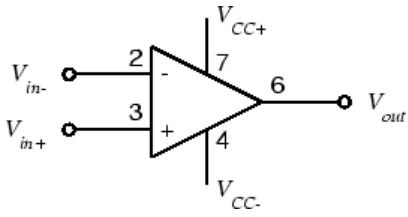
Output Stage :
This stage is normally a complementary output stage. It increases the magnitude of the voltage and raises the current supplying capability of OP-AMP.it also provides a low output resistance.



741 Op-amp

IC 741 Op Amp can provide high voltage gain and can be operated over a wide range of voltages; used in integrators, summing amplifiers and general feedback applications.

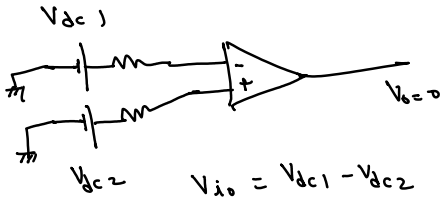




IDEAL OP-AMP CHARACTERISTICS

- Infinite Voltage gain
- Infinite input impedance
- Zero output impedance
- Zero output voltage when input is zero
- Infinite Bandwidth
- Infinite CMRR
- Infinite slew rate

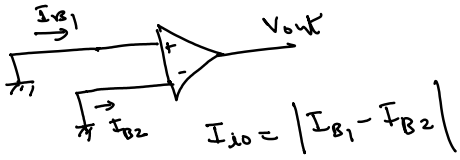
Typical Parameter values for 741 Op-amp



1. **Input Offset voltage**

   It is the voltage that must be applied between two input terminals of an op-amp to null the output.

   For 741C op-amp the maximum value of input offset voltage is 6mV dc.



2. **Input offset current**

   The algebraic difference between the currents into the inverting and non-inverting terminals is called input offset current

   The input offset current for 741C is 200nA maximum

3. **Input bias current**

   It is the average of the currents that flow into the inverting and non-inverting input terminals of the op-amp

   The maximum value for 741C is 500nA

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

4. **Differential input resistance**

   It is the equivalent resistance that can be measured at either inverting or non-inverting input with other terminal connected to ground.

   For 741C the input resistance is relatively high 2MΩ

5. **Input capacitance**

   It is the equivalent capacitance that can be measured at either inverting or non-inverting input with other terminal connected to ground.

   For 741C the input capacitance is 1.4pF

6. **Common Mode Rejection Ratio**

   It is the ratio of the differential voltage gain to the common mode gain.

$$CMRR = \frac{A_d}{A_{cm}}$$

   For 741C CMRR is typically 90dB

7. **Supply voltage Rejection Ratio**

   The change in an op-amps input offset voltage caused by variations in supply voltages is called SVRR.

   For 741C, SVRR is 6.31μV/V

8. **Large signal voltage gain**

$$\text{Voltage gain} = \frac{\text{Output Voltage}}{\text{differential input voltage}}$$

   For 741C it is typically 200000

9. **Output voltage swing**

For 741C output voltage swing is -13 and +13V

10. Output resistance

It is the equivalent resistance measured between the output and ground.

Typical value for 741C is 75Ω

11. Slew rate

It is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per microseconds.

$$SR = \left.\frac{dV_o}{dt}\right|_{max} \quad V/\mu S$$

One of the drawback of 741C is its low slew rate typically 0.5V/µS

12. Supply current

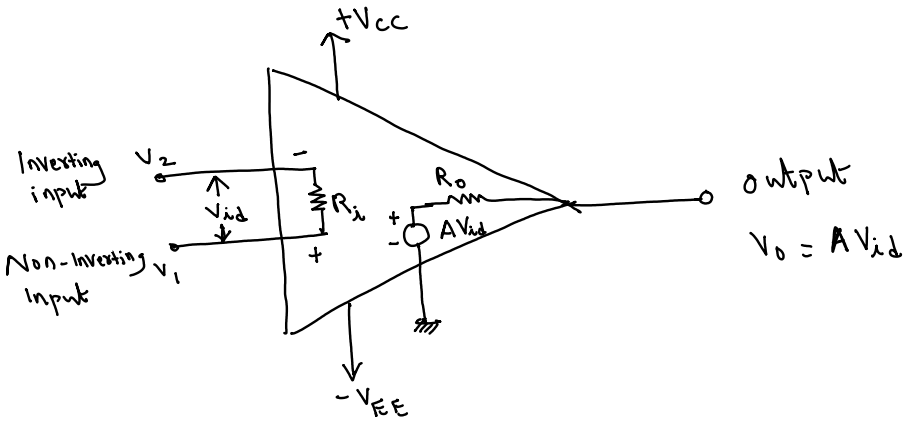
It is the current drawn by the op-amp from the power supply.

For 741C the supply current is 2.8mA

13. Power consumption

It is the amount of quiescent power that must be consumed by the op-amp in order to operate properly.
The amount of power consumed by 741C is 85mW.

Equivalent Circuit of an Op-amp



AV_{id} is equivalent Thevenin's voltage

R_o is the Thevenin's equivalent resistance

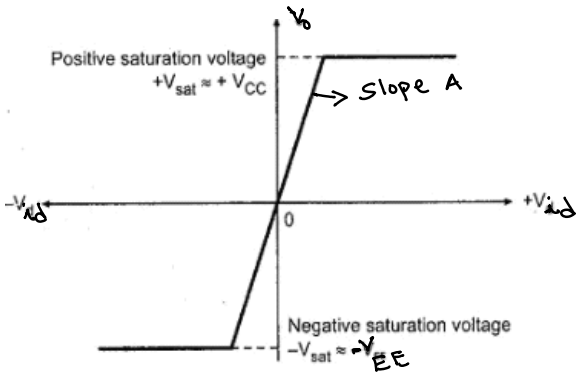
$V_o = AV_{id}$

$= A(V_1 - V_2)$

A → Large signal voltage gain.

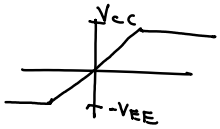
o/p amplifies the difference between the input signals.

Voltage transfer curve



$V_o = AV_{id}$

$V_o \propto V_{id}$

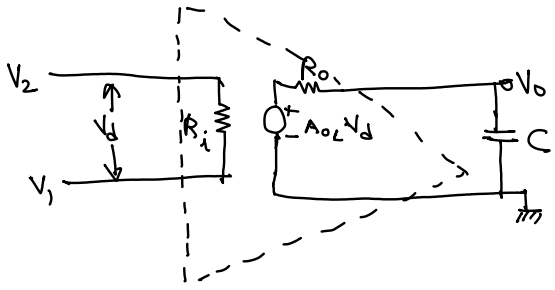


Output voltage is plotted against input difference voltage keeping gain A constant.

Output voltage cannot exceed the positive and negative saturation voltages.
These saturation voltages are specified by an output voltage swing rating of the op-amp for given values of supply voltages.
Output voltage is directly proportional to the input difference voltage only until it reaches the saturation voltages and thereafter output voltage remains constant.

This is known as ideal voltage transfer curve because output offset voltage is assumed to be zero.

Frequency response curve



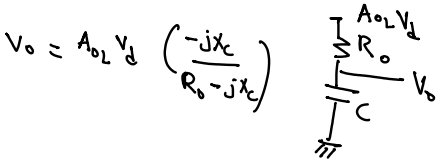


fig: High frequency model of an op-amp with single corner frequency.

Ideally an op-amp has infinite bandwidth.
This means that if its open-loop gain is 90dB with dc signal its gain should remain same 90dB through audio and high radio frequencies.
Practical op-amp gain decreases(roll-off) at higher frequencies.

There must be a capacitive component in the equivalent circuit of the op-amp.
This capacitance is due to the physical characteristics of the device used and the internal construction of the op-amp.

For a op-amp with only one break or corner frequency , all capacitor effects can be represented by a single capacitor C.

Here there is only one pole due to R_OC and a rolloff of -20dB/decade comes into effect.

$$V_o = A_{OL} V_d \left(\frac{-jX_c}{R_o - jX_c}\right)$$

$$A \simeq \frac{V_o}{V_d} \simeq A_{OL} \frac{\left(-j\frac{1}{2\pi fc}\right)}{\left(R_o - \frac{j}{2\pi fc}\right)}$$

$$\simeq A_{OL} \left(\frac{\frac{1}{j2\pi fc}}{R_o + \frac{1}{j2\pi fc}}\right)$$

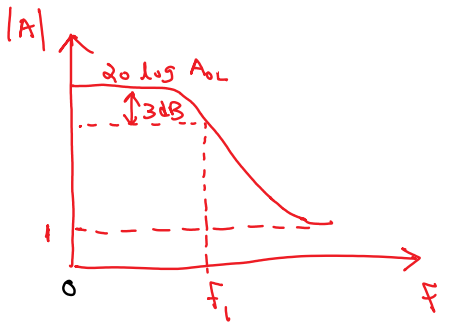
$$\simeq A_{OL} \frac{1}{1 + j2\pi f R_o c}$$

$$A \simeq \frac{A_{OL}}{1 + j\left(f/f_1\right)}$$

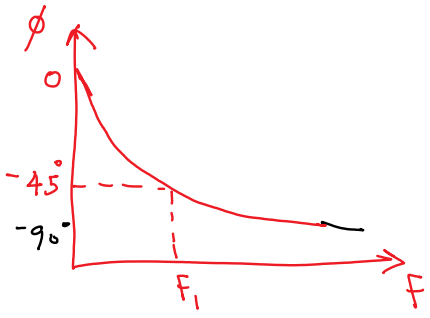
where $f_1 \simeq \frac{1}{2\pi R_o C}$ is the corner frequency

$$\text{magnitude } |A| \simeq \frac{A_{OL}}{\sqrt{1 + \left(f/f_1\right)^2}}$$

Phase $\phi = -\tan^{-1}\left(\frac{f}{f_1}\right)$



Magnitude characteristics



phase characteristics

magnitude chara

1) For frequencies $f << f_1$, the magnitude of gain is $20 \log A_{OL}$.

2) At $f = f_1$, the gain is 3dB down from dc value of A_{OL} in dB. This frequency is corner frequency.

3) for $f >> f_1$ the gain rolloff at -20dB/decade or -6dB/octave.

phase chara

1) The phase angle is zero at frequency 0.

2) At $f = f_1$, phase angle is -45° (lagging)

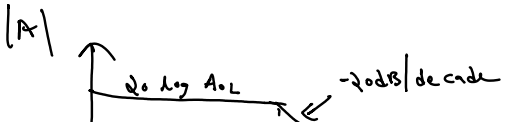
3) At infinite frequency, phase angle is -90°.

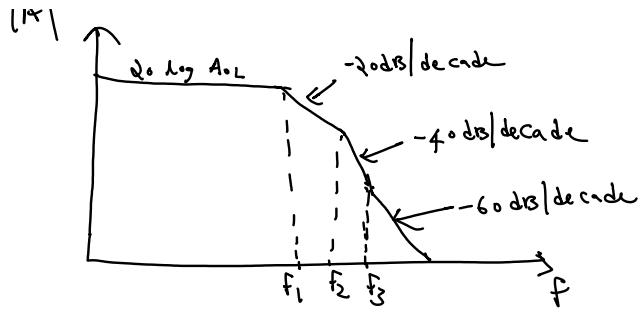
A practical op-amp has number of stages and each stage produces a capacitive component. Thus due to a number of RC pole pairs, their will be a number of different break frequencies.

Transfer function of op-amp with three corner frequencies

$$A = \frac{A_{OL}}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

$0 < f_1 < f_2 < f_3$




|A|
20 log A₀L
-20dB/decade
-40 dB/decade
-60 dB/decade
f₁
f₂
f₃
f

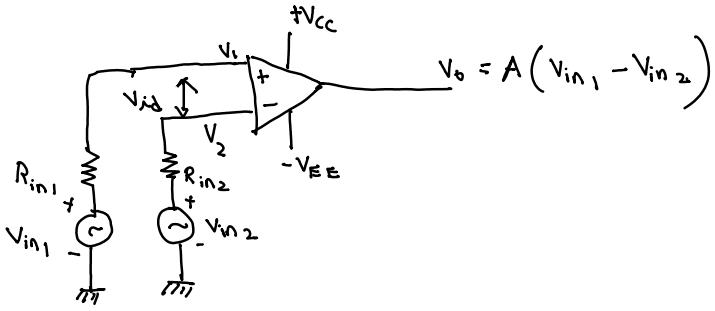
Open loop configuration

In the case of amplifiers, the term open loop indicates that no connection exists between input and output.
Output signal is not fed back in any form as part of the input signal.

When connected in open-loop configuration, the op-amp simply functions as a high gain amplifier.
There are three open-loop op-amp configurations:

1. Differential amplifier
2. Inverting amplifier
3. Non Inverting amplifier

Differential amplifier



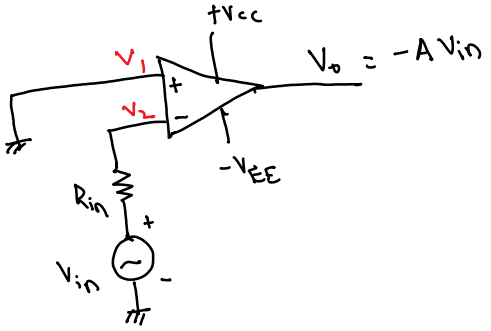
Since op-amp amplifies the difference between the input signals, this configuration is called differential amplifier.
This amplifier can amplify both ac and dc input signals.
The source resistances R_{in1} and R_{in2} are normally negligible compared to the input resistance R_i.
Therefore the voltage drop across these resistors can be assumed to be zero, which implies that $v_1 = V_{in1}$ and $v_2 = V_{in2}$

$$\therefore \quad V_o = A(V_{in1} - V_{in2})$$

In open loop configuration the gain A is commonly referred to as open-loop gain.
The polarity of the output depends on the polarity of the input difference voltage.

$$V_o = A(V_{id})$$
$$= A(V_1 - V_2)$$

Inverting amplifier



$$V_o = A(V_1 - V_2)$$
$$= A(0 - V_{in})$$
$$V_o = -AV_{in}$$

In the inverting amplifier only one input is applied and that is to the inverting terminal.
The non-inverting terminal is grounded.

Since $V_1 = 0\ V$

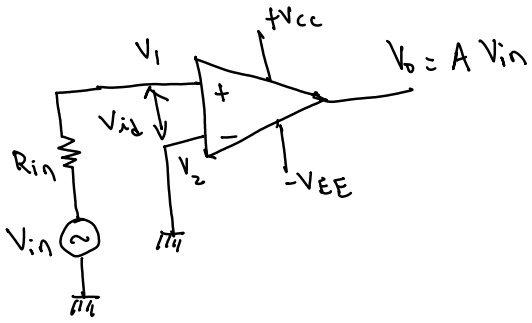
$V_2 = V_{in}$

$\therefore V_0 = A(V_1 - V_2) = A(0 - V_{in})$

$V_0 = -AV_{in}$

The negative sign indicates that the output voltage is out of phase with respect to input by 180^0

Non Inverting amplifier



$V_0 = A(V_1 - V_2)$

$= A(V_{in} - 0)$

$= AV_{in}$

In the non-inverting amplifier only one input is applied and that is to the non-inverting terminal. The inverting terminal is grounded.

$V_1 = V_{in}$

$V_2 = 0$

$\therefore V_0 = A(V_1 - V_2) = A(V_{in} - 0)$

$V_0 = AV_{in}$

output voltage is in phase with respect to input

When operated in open loop the output voltage is either positive or negative or switches between positive and negative saturation levels. So open-loop configurations are not used in linear amplifications.

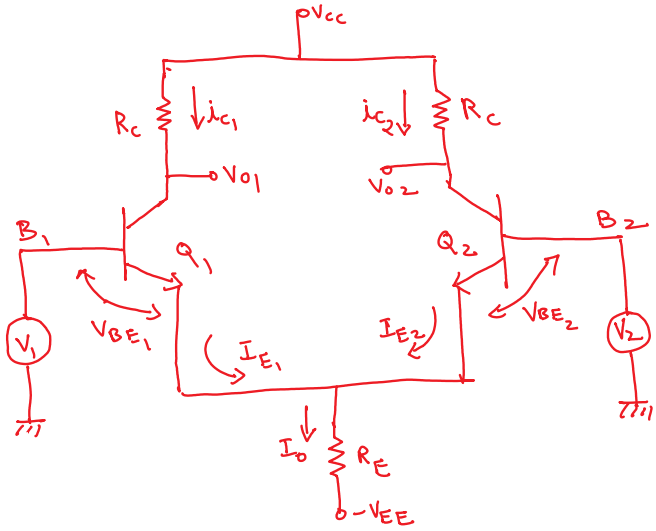
Differential amplifier

The differential amplifier is used to provide high gain to the difference mode signal and cancel the common mode signal.
Thus it is possible to suppress any signal common to both of the input terminals.
The relative sensitivity of an op-amp to a difference signal as compared to common mode signal is called common mode rejection ratio (CMRR) and gives the figure of merit of differential amplifier.
Higher the CMRR, better the op-amp.
Another requirement for op-amp is high input impedance.

$CMRR = \frac{A_d}{A_c}$

A cascade differential amplifier can provide high gain down to zero frequency as it has no coupling capacitor.
However such an amplifier suffer from the problem of drift of operating point due to temperature dependency of I_{CO}, V_{BE} and h_{fe} of the transistor.

This problem can be eliminated by using balanced or differential amplifier.

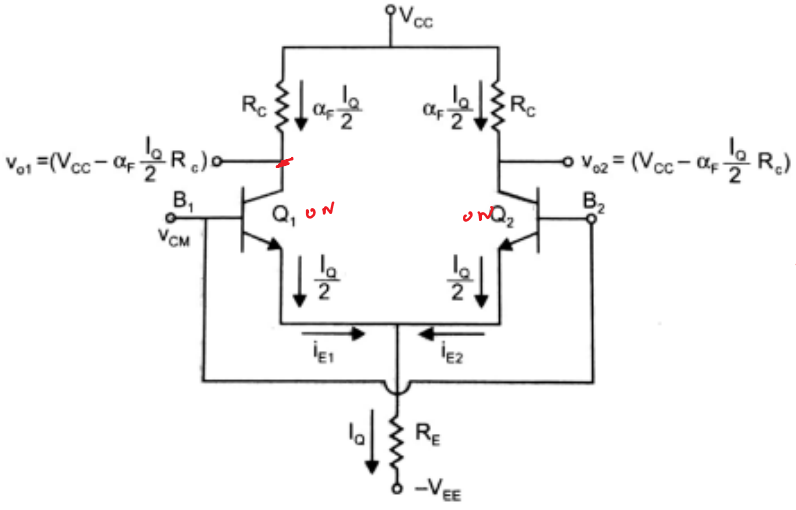


Differential amplifier

This circuit has low drift due to symmetrical construction and it can provide high input resistance.
B_2 is the inverting input and B_1 is the non-inverting input.

It can be used in four different configurations depending upon the number of input signals used and the way output is taken.

1. Differential input differential output or dual input balanced output
2. Differential input single ended output
3. Single input differential ~~output~~ output
4. Single input single ended output



$I_c = \alpha I_E$

$I_{c_1} = \alpha_F \frac{I_Q}{2}$

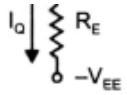
I_{c_2}

$V_{o1} = V_{cc} - I_{c_1} R_C$

$= V_{cc} - \alpha_F \frac{I_Q}{2} R_C$

$V_{o2} = V_{cc} - I_{c_2} R_C$

$= V_{cc} - \alpha_F \frac{I_Q}{2} R_C$



$V_{o2} = V_{CC} - I_{C_2} R_C$
$= V_{CC} - \alpha_F \frac{I_Q}{2} R_C$

Case 1

When $V_1 = V_2 = V_{cm}$ common mode voltage.

Here both transistors Q_1 and Q_2 are forward biased and matched due to symmetry of the circuit.

The current I_Q divides equally through transistors Q_1 and Q_2.

ie, $I_{E_1} = I_{E_2} = I_Q/2$

The collector current i_{c_1} and i_{c_2} through the resistors R_C is $\alpha_F I_Q/2$

The voltage at collectors V_{o1} and V_{o2} is $V_{CC} - \alpha_F \frac{I_Q}{2} R_C$

and therefore $V_{o1} - V_{o2}$ will be zero.

Thus even if the value of V_{cm} is changed, the voltage across collectors will not change.

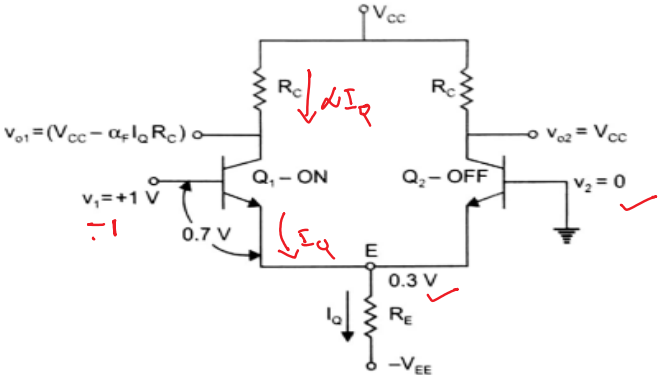
Thus the differential pair does not respond to (or rejects) the common mode input signals.

Case 2

When $V_2 = 0$ and $V_1 = 1V$

Q_1 will be ON Q_2 will be off

The entire I_Q will flow through Q_1



$V_{o1} = V_{CC} - I_C R_C$
$= V_{CC} - \alpha I_Q R_C$

$V_{BE} = 0.7$
$V_B - V_E = 0.7$
$0 - V_E = 0.7$
$V_E = 0.3$

Since Q_1 is on, the voltage at emitter will be 0.3V

This will make Q_2 reversed biased or Q_2 is off.

$$\therefore V_{o1} = V_{CC} - \alpha_F I_Q R_C$$

$$V_{o2} = V_{CC}$$

If $V_1 = -1V$ and $V_2 = 0V$ Q_1 will be off and the entire current I_Q will flow through Q_2.

The voltage at E will be $-0.7V$ which make Q_1 OFF and Q_2 ON.

$$V_{o1} = V_{CC}$$

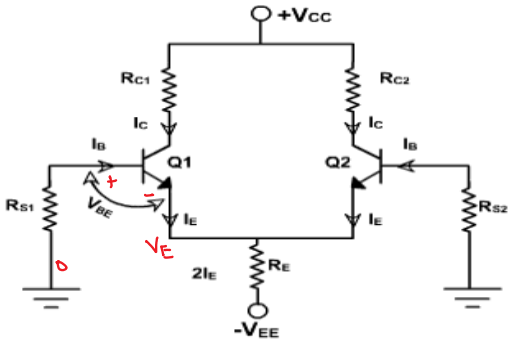
$$V_{o2} = V_{CC} - \alpha_F I_Q R_C$$

Thus the differential amplifier responds only to the difference mode signals and rejects Common mode signals.

DC Analysis of Differential Amplifier

The dc analysis means to obtain the operating point values i.e. I_{CQ} and V_{CEQ} for the transistors used.

To obtain the operating point (I_{CQ} and V_{CEQ}) for differential amplifier dc equivalent circuit is drawn by reducing the input voltages v_1 and v_2 to zero.



$0 - V_E = V_{BE}$

$V_E = -V_{BE}$

The internal resistances of the input signals are denoted by R_S because $R_{S1} = R_{S2}$.
Since both emitter biased sections of the different amplifier are symmetrical in all respects, therefore, the operating point for only one section need to be determined.
The same values of I_{CQ} and V_{CEQ} can be used for second transistor Q2.

Apply KVL to the base emitter loop of Q_1

$$I_B R_S + V_{BE} + 2I_E R_E = V_{EE}$$

$I_C \simeq I_E$

$I_B = \frac{I_E}{\beta}$

$$R_S \frac{I_E}{\beta} + V_{BE} + 2I_E R_E = V_{EE}$$

$$\left(\frac{R_S}{\beta} + 2R_E\right) I_E = V_{EE} - V_{BE}$$

$$I_C \simeq I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E}$$

Since $\frac{R_S}{\beta} << 2R_E$

$$I_C = I_E \simeq \frac{V_{EE} - V_{BE}}{2R_E} \longrightarrow (1)$$

I_E is independant of R_C

$$V_C = V_{CC} - I_C R_C$$

We have $V_{CE} = V_C - V_E$

$$= V_{CC} - I_C R_C - V_E \quad \checkmark$$

Neglecting the voltage drop across R_s, the voltage across emitter $V_E = -V_{BE}$

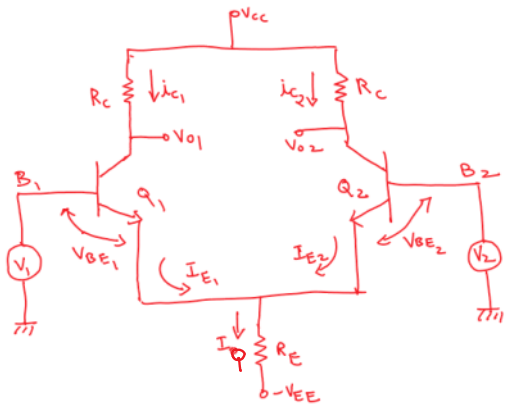
$$V_{CE} = V_{CC} - I_C R_C + V_{BE} \quad \rightarrow (2)$$

$$I_E = I_C = I_{CQ}$$

$$V_{CE} = V_{CEQ}$$

$(2) \Rightarrow V_{CEQ} = V_{CC} - I_{CQ} R_C + V_{BE}$

Transfer characteristics of differential amplifier



Assumptions

1) $R_s = 0$
2) Constant current source o/p resistance is infinity.

$$i = I_s e^{\eta v / \eta_T}$$

$$V_T = \frac{K_T}{q}$$

The collector currents i_{c_1} and i_{c_2} of the two matched transistors in forward active mode given by

$$i_{c_1} = I_s e^{V_{EB_1}/V_T} \rightarrow (1)$$

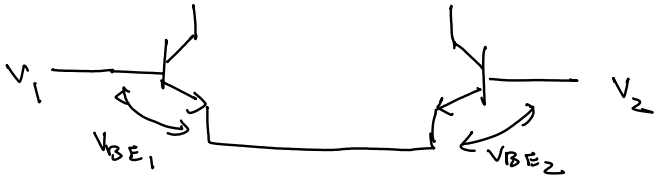
$$i_{c_2} = I_s e^{V_{EB_2}/V_T} \rightarrow (2)$$

where I_s is reverse leakage current.

$(1)/(2)$

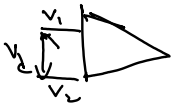
$$\frac{i_{c_1}}{i_{c_2}} = \frac{e^{V_{EB_1}/V_T}}{e^{V_{EB_2}/V_T}}$$

$$\frac{i_{c_1}}{i_{c_2}} = e^{(V_{EB_1} - V_{EB_2})/V_T} \rightarrow (3)$$



KVL

$$V_1 - V_{BE_1} + V_{BE_2} - V_2 = 0$$



$$V_{BE_1} - V_{BE_2} = V_1 - V_2 = V_d \rightarrow (4)$$

From fig, $I_Q = i_{E_1} + i_{E_2}$

$$= \frac{i_{c_1}}{\alpha_T} + \frac{i_{c_2}}{\alpha_T}$$

$$= \frac{i_{c_1}}{} \left(1 + \frac{i_{c_2}}{}\right) \rightarrow (5)$$

$$i_{c_1} = \alpha_T i_{E_1}$$

$$= \frac{i_{C_1}}{\alpha_T}\left(1 + \frac{i_{C_2}}{i_{C_1}}\right) \quad \hookrightarrow (5)$$

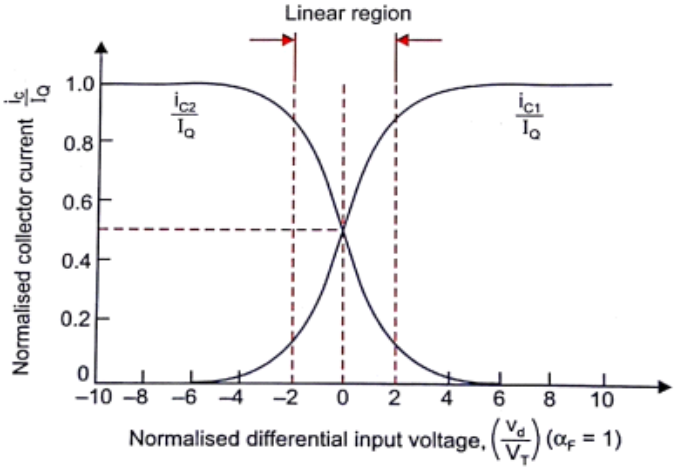
$(3) \Rightarrow \quad \frac{i_{C_1}}{i_{C_2}} = e^{V_d/V_T}$

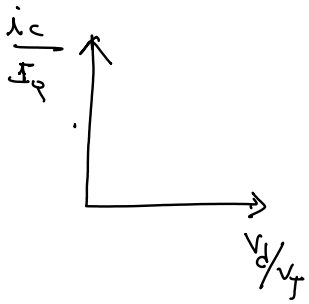
$$\frac{i_{C_2}}{i_{C_1}} = \frac{1}{e^{V_d/V_T}} = e^{-V_d/V_T}$$

$\therefore (5) \Rightarrow \quad I_Q = \frac{i_{C_1}}{\alpha_T}\left(1 + e^{-V_d/V_T}\right)$

$$\boxed{i_{C_1} = \frac{\alpha_T I_Q}{1 + e^{-V_d/V_T}}}$$

$$\boxed{i_{C_2} = \frac{\alpha_T I_Q}{1 + e^{V_d/V_T}}}$$





a) for $V_d > +V_T$ $\quad i_{c_1} = \alpha I_Q$ and $i_{c_2} = 0$

$$V_{o_1} = V_{cc} - \alpha I_Q R_c$$

$$V_{o_2} = V_{cc}$$

By proper value of R_c V_{o_1} can be made very small

b) For $V_d < -V_T$ $\quad i_{c_1} = 0$ and $i_{c_2} = \alpha I_Q$

$$V_{o_1} = V_{cc}$$

V_{o_2} is negligible

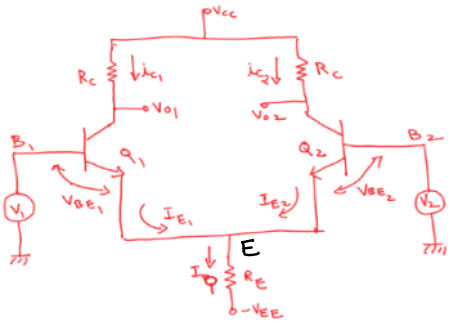
Thus for $+V_T < V_d < -V_T$ the differential amplifier can be made to operate as a switch.

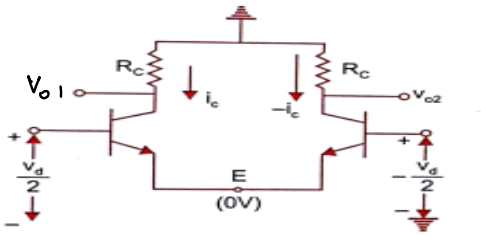
c) The differential amplifier can be made to operate as a limiter for $V_d > \pm V_T$

d) The differential amplifier can function as AGC by varying I_Q.

e) Between $-2V_T \leq V_d \leq 2V_T$, the differential amplifier can operate as a linear amplifier.

AC analysis of Differential amplifier using hybrid π model





For $V_1 = V_2$ the current I_Q divides equally into the transistors because of the symmetry of the circuit.

If V_1 is now increased by $V_d/2$ and V_2 is decreased by $V_d/2$ the differential Amplifier is being fed by differential small signal V_d.

The common mode signal is zero.

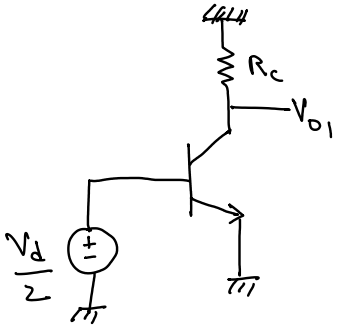
The collector current i_{c_1} will increase by i_c and i_{c_2} will decrease by i_c.

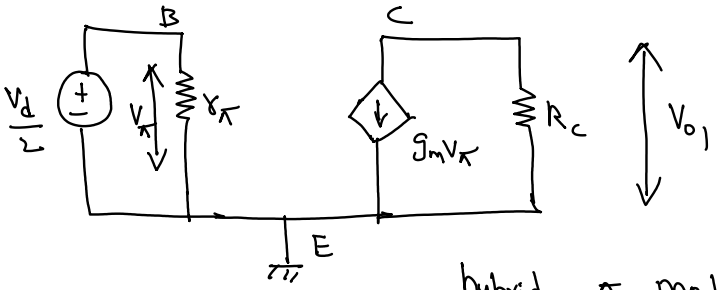
The sum of total currents through Q_1 and Q_2 remains constant as constrained by constant current I_Q.

As there is no change of current through R_E, Voltage V_E remains constant.

∴ For small signal analysis, E can be considered to be at ground potential

Since both sides performance of a differential amplifier are identical, consider differential half circuit.





hybrid π model

$$V_{o1} = (-g_m V_\pi) R_C$$

$$= -g_m \left(\frac{V_d}{2}\right) R_C$$

$$\frac{V_{o1}}{V_d} = -\frac{1}{2} g_m R_C$$

$$\text{III}^{\text{rly}} \quad \frac{V_{o2}}{V_d} = \frac{1}{2} g_m R_C$$

If o/p is taken differentially, the differential gain

$$A_{DM} = \frac{V_{o1} - V_{o2}}{V_d} = -\tfrac{1}{2} g_m R_C - \tfrac{1}{2} g_m R_C$$

$$\boxed{A_{DM} = -g_m R_C} \quad \rightarrow (1)$$

(Differential input Differential output)

If o/p is single ended

$$A_{DM} = \frac{V_{o1}}{V_d} = -\tfrac{1}{2} g_m R_C$$

and $$\frac{V_{o2}}{V_d} = \tfrac{1}{2} g_m R_C$$

If o/p resistance r_o is considered.

$(1) \Rightarrow$ $$A_{DM} = -g_m (R_C \| r_o)$$

Common mode Gain A_{cm}

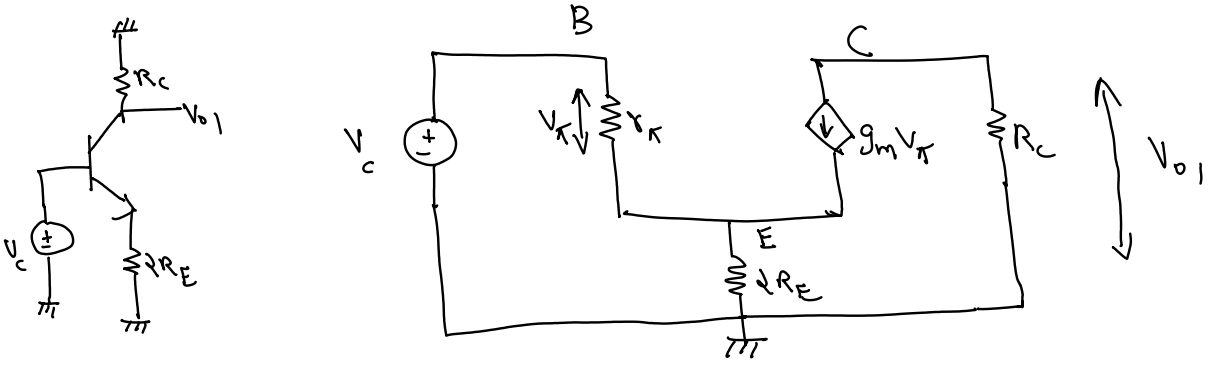
When both V_1 and V_2 are increased by a voltage V_c, the differential signal V_d is zero and common mode signal is V_c.

Both collector current increases by i_c

The current through R_E increases by $2i_c$.

Voltage at emitter is increased by $2i_cR_E$ and no longer constant.

Draw the common mode half circuit with R_E replaced by $2R_E$



$$V_c = I_B\left(r_\pi + 2R_E(1+\beta)\right)$$

$$A_{cm} = \frac{V_{o1}}{V_c} = \frac{(-g_mV_\pi)R_C}{I_B\left(r_\pi + 2R_E(1+\beta)\right)}$$

$$= \frac{-I_cR_C}{I_B\left(r_\pi + 2R_E(1+\beta)\right)}$$

$$= \frac{-\beta I_BR_C}{I_B\left(r_\pi + 2R_E(1+\beta)\right)}$$

$$= \frac{-\beta R_C}{r_\pi + 2R_E(1+\beta)} \quad \hookrightarrow (1)$$

(1) $\Rightarrow$ $A_{cm} = \dfrac{-\beta R_C}{r_\pi + 2R_E(1+\beta)}$

For $\beta >> 1$

(since r_π is small)

$$A_{cm} = \frac{-\beta R_C}{2R_E(1+\beta)}$$

$r_\pi + 2R_E(1+\beta)$ $\qquad$ $2R_E(1+\beta)$

For $\beta > 1$ $\qquad$ For $\beta >> 1$

$$A_{cm} = \frac{-\beta R_C}{r_\pi + 2R_E\beta} \qquad A_{cm} \simeq \frac{-\beta R_C}{2R_E\beta}$$

$$= \frac{-R_C}{2R_E}$$

But $\beta = g_m r_\pi$

$$\therefore A_{cm} = \frac{-g_m r_\pi R_C}{r_\pi + 2R_E g_m r_\pi}$$

$$\boxed{A_{cm} = \frac{-g_m R_C}{1 + 2g_m R_E}} \longrightarrow (2)$$ for single ended o/p

CMRR

$$CMRR = \left| \frac{A_{DM}}{A_{CM}} \right|$$

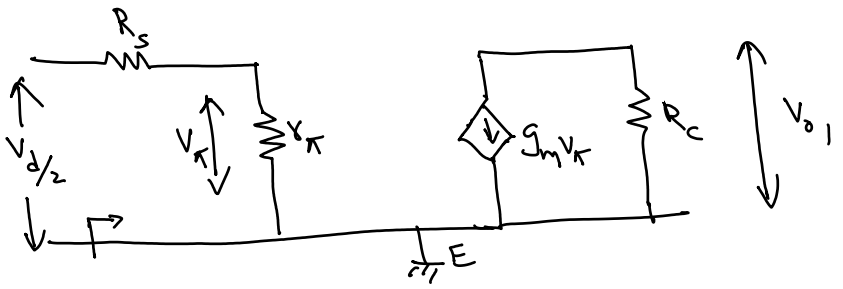
$$= \frac{g_m R_C}{g_m R_C / 1 + 2g_m R_E}$$

$$= 1 + 2g_m R_E$$

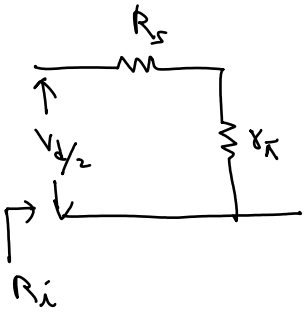
$$CMRR \simeq 2g_m R_E$$

Input and output resistance

Considering R_s



Input resistance R_i



$$V_{d/2} = I_B (R_s + r_\pi)$$

$$R_i = \frac{V_d}{I_B} = 2 (R_s + r_\pi)$$

o/p resistance

$$R_o = R_c$$

Constant current bias

For CMRR to be large, A_c should be as small as possible.

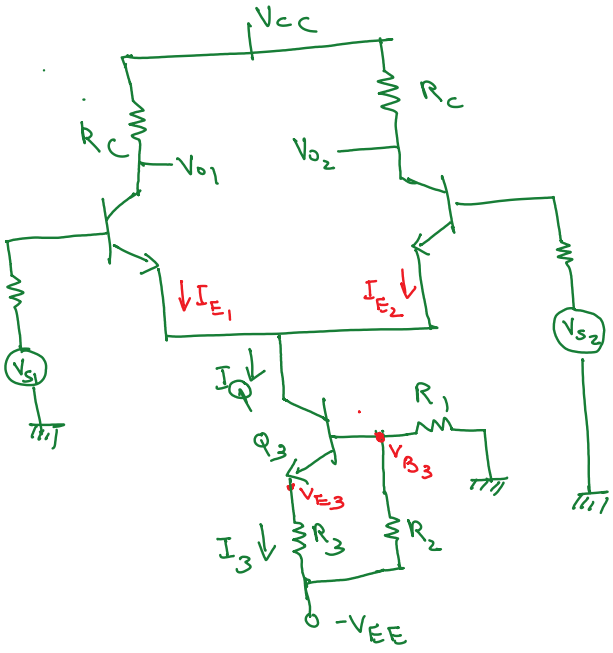
$A_c \to 0$ as $R_E \to \infty$ $\qquad CMRR = \frac{A_d}{A_c}$

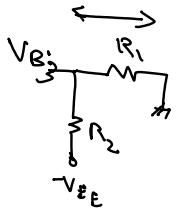
If R_E is made large, the emitter supply will also have to be increased in order to maintain the proper quiescent current.

If the operating currents of the transistors are allowed to decrease, then h_{fe} will decrease.

This too will decrease the CMRR.

The use of constant current bias in place of R_E is a practical solution to this problem.





$V_{BE_3} = V_{B_3} - V_{E_3}$

R_E is replaced by a constant current transistor circuit in which R_1, R_2 and R_3 can be adjusted to give the same quiescent conditions for the transistors Q_1 and Q_2 as in the original circuit. The modified circuit presents a very high effective emitter resistance R_E even for very small values of R_3.

We have $I_3 = \dfrac{V_{E_3} - (-V_{EE})}{\quad}$

$$= \frac{V_{E3} + V_{EE}}{R_3} \quad \hookrightarrow (1)$$

Also, $V_{BE_3} = V_{B3} - V_{E3} \quad \hookrightarrow (2)$

$$V_{B3} = -V_{EE} \frac{R_1}{R_1 + R_2} \quad \hookrightarrow (3)$$

Substitute (3) in (2)

$$V_{BE_3} = -V_{EE} \frac{R_1}{R_1 + R_2} - V_{E3}$$

$$V_{E3} = -V_{EE} \frac{R_1}{R_1 + R_2} - V_{BE_3}$$

Substitute V_{E3} in eqn (1)

$$\therefore I_3 = \frac{-V_{EE} \frac{R_1}{R_1 + R_2} - V_{BE_3} + V_{EE}}{R_3} \quad \rightarrow (4)$$

From fig, $\boxed{I_3 \approx I_Q}$

The current I_Q is constant as it does not depend on signal voltages V_{s1} and V_{s2}.

With I_Q constant, common mode gain is zero so that the circuit provides high CMRR.

$$I_Q = I_{E_1} + I_{E_2}$$

If $I_{E_1} = I_{E_2}$

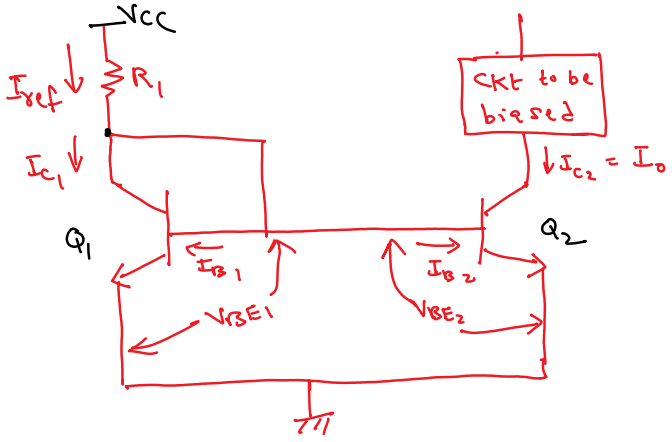
$$I_Q = 2 I_{E_1}$$

(4) $\Rightarrow$

$$2 I_{E_1} = \frac{-V_{EE} \frac{R_2}{R_1 + R_2} - V_{BE_3} + V_{EE}}{R_3}$$

$$I_{E_1} = \frac{-V_{EE} \frac{R_2}{R_1 + R_2} - V_{BE_3} + V_{EE}}{2R_3}$$

Constant Current source(Current mirror)



A constant current source make use of the fact that for a transistor in the active mode of operation, the collector current is independent of the collector voltage.

Q_1 and Q_2 are matched transistors.

Q_1 is connected as diode by shorting collector to its base.

since Q_1 and Q_2 are matched, the emitter current of Q_2 will be equal to emitter current of Q_1 which is approximately equal to I_{ref}.

As long as Q_2 is maintained in active mode of operation,

$I_{C_2} = I_o \approx I_{ref}$.

Since output current I_o is a reflection or mirror of the reference current I_{ref}, the circuit is refferred to as Current mirror.

Analysis

$$I_{C_1} = \alpha_F I_{ES} e^{V_{BE_1}/V_T}$$

$$I_{C_2} = \alpha_F I_{ES} e^{V_{BE_2}/V_T}$$

$$\frac{I_{C_2}}{I_{C_1}} = e^{(V_{BE_2} - V_{BE_1})/V_T}$$

Since $V_{BE_1} = V_{BE_2}$

$$I = I_s e^{V/V_T}$$

$$V_T = \frac{KT}{q}$$

$$\frac{I_{C_2}}{I_{C_1}} = e^{0} = 1$$

$$\therefore \quad I_{C_2} = I_{C_1} = I_C = I_o$$

Since both transistors are identical

$$\beta_1 = \beta_2 = \beta$$

Apply KCL at the collector node of Q_1

$$I_{ref} = I_{C_1} + I_{B_1} + I_{B_2}$$

$$= I_{C_1} + \frac{I_{C_1}}{\beta_1} + \frac{I_{C_2}}{\beta_2}$$

$$= I_C \left(1 + \frac{1}{\beta} + \frac{1}{\beta}\right)$$

$$I_{ref} = I_C \left(1 + \frac{2}{\beta}\right)$$

$$I_C = \frac{\beta}{\beta+2} I_{ref} \longrightarrow (1)$$

where $I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \simeq \frac{V_{CC}}{R_1}$ V_{BE} small

For $\beta >> 1$

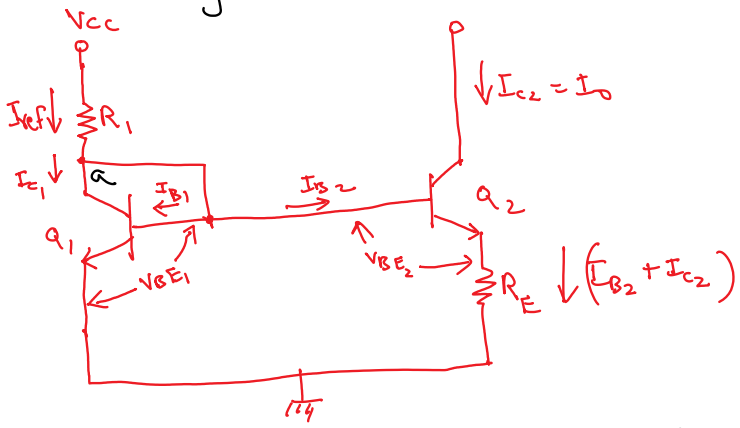
eqn (1)

$\Rightarrow \frac{\beta}{\beta+2}$ is almost unity

$$\therefore I_C = I_{ref}$$

Widlar Current mirror

The basic current mirror has a limitation. whenever we need a low value current source, the value of resistance R_1 is sufficiently high and cannot be fabricated economically.



This widlar current mirror is suitable for low value current source.

The only difference in this circuit is R_E is included in emitter of Q_2.

$$\therefore V_{BE_2} < V_{BE_1}$$

I_o is smaller than I_{C_1}.

$$\frac{I_{C_1}}{I_{C_2}} = e^{(V_{BE_1} - V_{BE_2})/V_T}$$

Take natural log

$$\ln \frac{I_{C_1}}{I_{C_2}} = \frac{V_{BE_1} - V_{BE_2}}{V_T}$$

$$V_{BE_1} - V_{BE_2} = V_T \ln \frac{I_{C_1}}{I_{C_2}} \longrightarrow (1)$$

Apply KVL to emitter base loop

$$V_{BE_1} = V_{BE_2} + (I_{B_2} + I_{C_2})R_E$$

$$V_{BE_1} - V_{BE_2} = (I_{B_2} + I_{C_2}) R_E$$

$I_C = \beta I_B$

$I_B = \frac{I_C}{\beta}$

$$= \left(\frac{I_{C_2}}{\beta} + I_{C_2}\right) R_E$$

$$= \left(\frac{1}{\beta} + 1\right) I_{C_2} R_E$$

$$\therefore (1) \Rightarrow \left(\frac{1}{\beta} + 1\right) I_{C_2} R_E = V_T \ln \left(\frac{I_{C_1}}{I_{C_2}}\right)$$

$$R_E = \frac{V_T}{\left(1+\frac{1}{\beta}\right) I_{C_2}} \ln\left(\frac{I_{C_1}}{I_{C_2}}\right)$$

At node a,

Apply KCL

$$I_{ref} = I_{C_1} + I_{B_1} + I_{B_2}$$

$$= I_{C_1} + \frac{I_{C_1}}{\beta} + \frac{I_{C_2}}{\beta}$$

$$= I_{C_1}\left(1+\frac{1}{\beta}\right) + \frac{I_{C_2}}{\beta} \quad \Rightarrow (2)$$

In widlar current source

$$I_{C_2} << I_{C_1}$$

$\therefore \frac{I_{C_2}}{\beta}$ can be neglected

$$(2) \Rightarrow I_{ref} \simeq I_{C_1}\left(1+\frac{1}{\beta}\right)$$

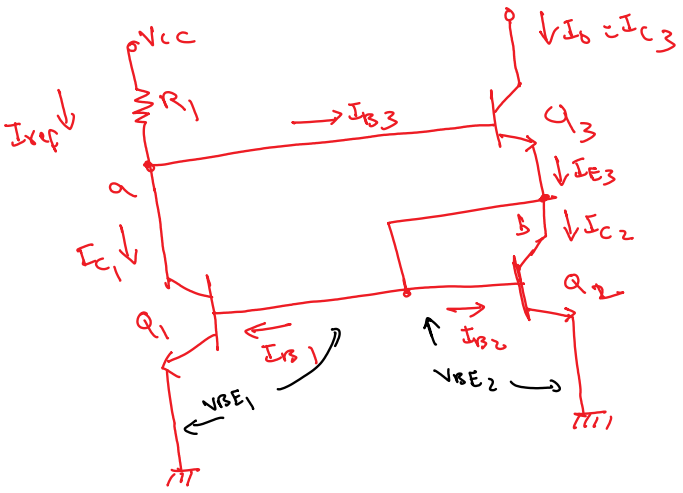
$$I_{C_1} \simeq \frac{\beta}{\beta+1} I_{ref}$$

where $I_{ref} \simeq \frac{V_{CC} - V_{BE_1}}{R_1}$

For $\beta >> 1$

$$I_{C_1} \simeq I_{ref}$$

Wilson Current Mirror



This current source provides an output current I_o which is very nearly equal to I_{ref} and also exhibits a very high output resistance.

We have $V_{BE_1} = V_{BE_2}$

$I_{C_1} = I_{C_2}$ and $I_{B_1} = I_{B_2} = I_B$

At node b, apply KCL

$$I_{E_3} = I_{C_2} + I_{B_1} + I_{B_2}$$

$$= I_{C_2} + 2I_B$$

$$= I_{C_2} + 2\frac{I_{C_2}}{\beta}$$

$$= I_{C_2}\left(1 + \frac{2}{\beta}\right) \quad \rightarrow (1)$$

$I_C = \beta I_B$

$I_B = \frac{I_C}{\beta}$

Also $I_{E_3} = I_{C_3} + I_{B_3}$ $\rightarrow (2)$

$$= I_{C_3} + \frac{I_{C_3}}{\beta} = I_{C_3}\left(1 + \frac{1}{\beta}\right)$$

Equating (1) and (2)

$$I_{C_3}\left(1 + \frac{1}{\beta}\right) = I_{C_2}\left(1 + \frac{2}{\beta}\right)$$

$$I_{C_3}\left(\frac{\beta+1}{\beta}\right) = I_{C_2}\left(\frac{\beta+2}{\beta}\right)$$

✓ $I_o = I_{C_3} = \left(\frac{\beta+2}{\beta+1}\right) I_{C_2}$

$$I_o = I_{C_3} = \left(\frac{\beta+2}{\beta+1}\right) I_{C_2}$$

Since $I_{C_1} = I_{C_2}$

$$I_o = \left(\frac{\beta+2}{\beta+1}\right) I_{C_1} \longrightarrow (3)$$

At node a,

$$I_{ref} = I_{C_1} + I_{B_3}$$

$$= \left(\frac{\beta+1}{\beta+2}\right) I_o + \frac{I_o}{\beta}$$

$$= I_o \left[\frac{\beta^2+\beta+\beta+2}{\beta(\beta+2)}\right]$$

$$I_{ref} = I_o \left[\frac{\beta^2+2\beta+2}{\beta^2+2\beta}\right]$$

$$I_o = \frac{\beta^2+2\beta}{\beta^2+2\beta+2} I_{ref}$$

$I_o = I_{C_3} = \beta I_{B_3}$

$I_{B_3} = \frac{I_o}{\beta}$

where $I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_1}$

$$I_o - I_{ref} = \frac{2}{\beta^2+2\beta+2} I_{ref}$$

The difference $I_o - I_{ref}$ is extremely small error for modest values of β.

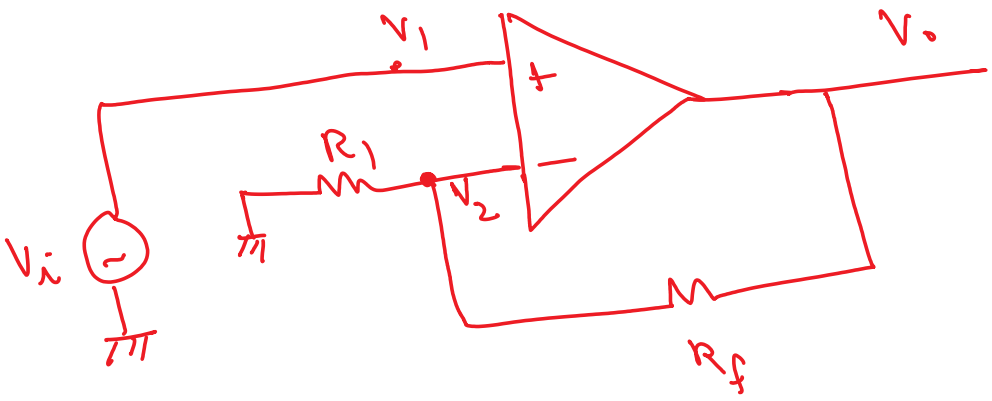
The o/p resistance of wilson current mirror is greater ($\equiv \frac{\beta r_o}{2}$) than simple current mirror or widlar current mirror

Module 2:

Op-amp with negative feedback: General concept of Voltage Series, Voltage Shunt, current series and current shunt negative feedback, Op Amp circuits with voltage series and voltage shunt feedback, Virtual ground Concept; analysis of practical inverting and non-inverting amplifiers for closed loop gain, Input Resistance and Output Resistance.

Op-amp applications: Summer, Voltage Follower-loading effects, Differential and Instrumentation Amplifiers, Voltage to current and Current to voltage converters, Integrator, Differentiator, Precision rectifiers, Comparators, Schmitt Triggers, Log and antilogamplifiers.

Closed loop gain of practical non inverting op-amp



$$V_d = V_1 - V_2$$

$$= V_i - V_o \frac{R_1}{R_1 + R_f}$$

Let $B = \frac{R_1}{R_1 + R_f}$

$$V_d = V_i - V_o B \quad \longrightarrow (1)$$

we have $A_{OL} = \frac{V_o}{V_d}$

$$V_o = A_{OL} V_d$$

$$V_o = A_{OL}(V_i - V_o B)$$

$$V_o (1 + A_{OL} B) = V_i A_{OL}$$

$$A_{CL} = \frac{V_o}{V_i} = \frac{A_{OL}}{1 + A_{OL} B}$$

Concept of feedback in op-amp

Because the open-loop gain of the op-amp is very high, only the smaller signals having very low frequency may be amplified accurately without distortion.
Open-loop gain is not a constant, the voltage gain varies with with changes in temperature and power supply and other production techniques.
The bandwidth of most open-loop op-amps is negligible small.
Open loop op-amp is not used in linear applications.

By the use of Feedback, an output signal is fed back to the input either directly or via another network.
If signal fed back is of opposite polarity or out of phase by 180 degree w.r.t the input signal, the feedback is known as negative feedback or degenerative feedback. It degenerates the output voltage amplitude and in turn reduces the voltage gain.
If the signal fed back is of same phase or in same polarity with the input signal, the feedback is called positive feedback or regenerative feedback. Positive feedback is used in Oscillators.

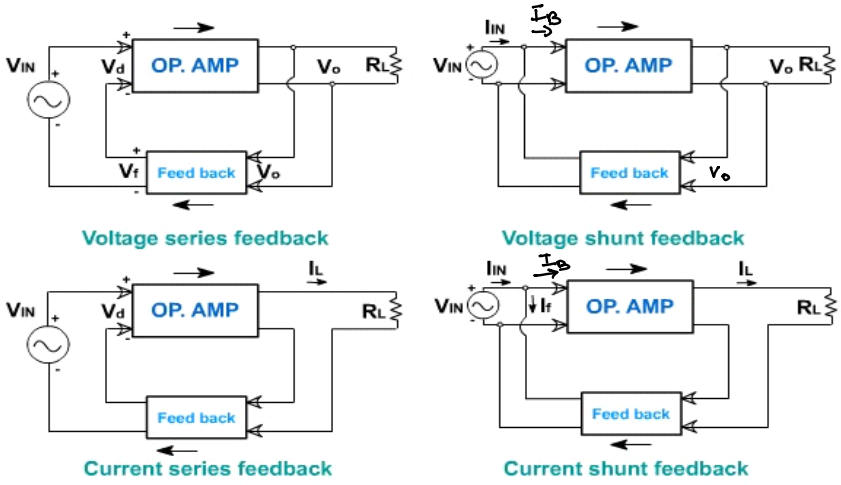
When used in amplifiers, negative feedback stabilizes gain, increases the bandwidth and changes the input and output resistances. But voltage gain will be reduced.
It decreases harmonic distortion and reduction in the effect of input offest voltage at the output, reduces the effect of variations in temperature and power supply voltage on the output of the op-amp.

Classification

An op-amp that uses feedback is called a feedback amplifier.
A feedback amplifier is sometimes referred to as a closed loop amplifier.
A feedback amplifier consists of two parts- an op-amp circuit and a feedback circuit.

There are four ways of connecting these two blocks.
These connections are classified according to whether the voltage or current is fed back to the input in series or in parallel

1. Voltage-series feedback
2. Voltage-shunt feedback
3. Current-series feedback
4. Current-shunt feedback



In voltage series and voltage shunt feedback, the voltage across R_L is the input voltage to the feedback circuit. The feedback quantity (either voltage or current) is the output of the feedback circuit is proportional to the output voltage

In current series and current shunt feedback, the current i_L flows into the feedback circuit. The output of the feedback circuit (either voltage or current) is proportional to load current i_L.

Voltage- Series Feedback

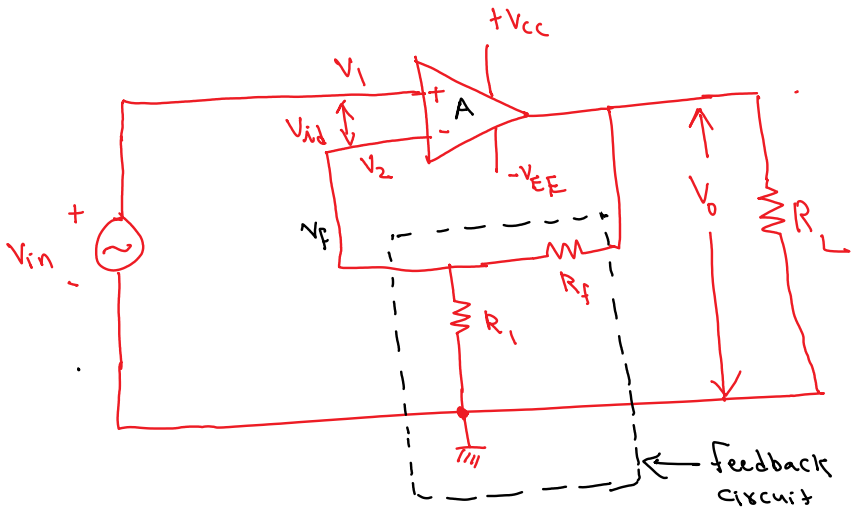
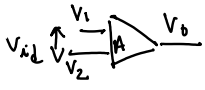


fig: Non-Inverting amplifier with voltage series feedback.

The op-amp circuit includes op-amp with large signal voltage gain A, feedback circuit with two resistors R_1 and R_f.

Openloop voltage gain (gain without feedback)

$$A = \frac{V_o}{V_{id}}$$



Closed loop voltage gain (Gain with feedback)

$$A_F = \frac{V_o}{V_{in}}$$

Gain of the feedback circuit $B = \frac{V_f}{V_o}$

Negative feedback

$$V_{id} = V_{in} - V_f$$

This shows the feedback voltage always opposes the input voltage (or out of phase by 180°), feedback is always negative.

Closed loop Voltage Gain

Closed loop voltage gain

$$A_F = \frac{V_o}{\quad} \rightarrow (1)$$

V_{in}

We have $V_o = A(V_1 - V_2)$ → (2) $A = \frac{V_o}{V_1 - V_2}$

Here $V_1 = V_{in}$

$$V_2 = V_f = V_o \frac{R_1}{R_1 + R_f}$$

$$\therefore (2) \Rightarrow V_o = A\left(V_{in} - V_o \frac{R_1}{R_1 + R_f}\right)$$

$$V_o = \frac{A(R_1 + R_f)V_{in}}{R_1 + R_f} - \frac{A V_o R_1}{R_1 + R_f}$$

$$V_o\left(1 + \frac{AR_1}{R_1 + R_f}\right) = \frac{A(R_1 + R_f)V_{in}}{R_1 + R_f}$$

Closed loop gain

$$\therefore A_f = \frac{V_o}{V_{in}} = \frac{A(R_1 + R_f)}{R_1 + R_f + AR_1} \rightarrow (3) \quad (\text{exact})$$

Since A is very large

$$AR_1 >> R_1 + R_f$$

$$(3) \Rightarrow \therefore A_F = \frac{A(R_1 + R_f)}{AR_1} = \frac{R_1 + R_f}{R_1}$$

$$= 1 + \frac{R_f}{R_1} \quad (\text{ideal}) \hookrightarrow (4)$$

We also have

Feedback circuit gain $B = \frac{V_f}{V_o} = \frac{R_1}{R_1 + R_f}$ → (5)

comparing (4) and (5)

$$\boxed{A_f = \frac{1}{\beta}}$$

From (3)

$$A_f = \frac{A(R_1 + R_f)}{R_1 + R_f + AR_1}$$

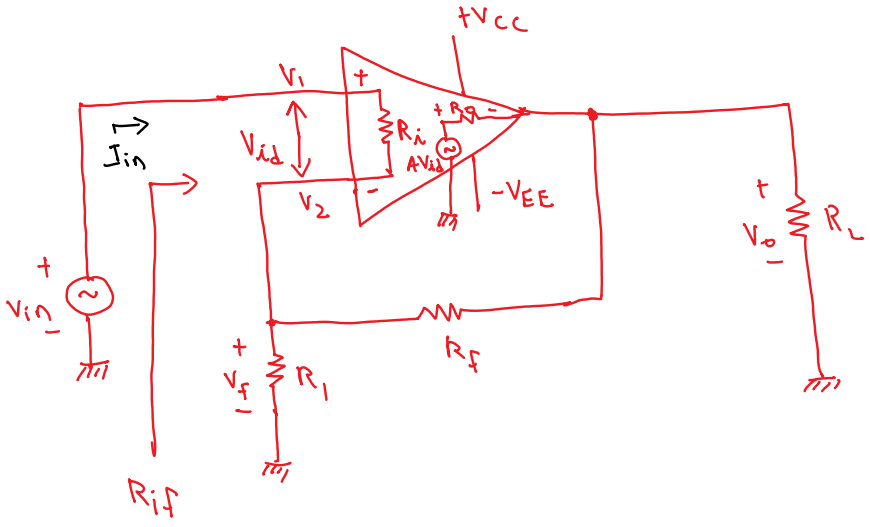
$$\simeq \frac{A\,\dfrac{(R_1+R_f)}{R_1+R_f}}{\dfrac{R_1+R_f}{R_1+R_f} + A\dfrac{R_1}{R_1+R_f}} = \frac{A}{1+AB}$$

Closed loop gain

$$\boxed{A_F \simeq \frac{A}{1+AB}}$$

AB is loop gain

Input resistance with feedback

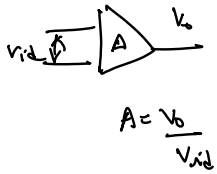


R_i is the input resistance of the op-amp

R_{if} is the input resistance with feedback

$$R_{if} \simeq \frac{V_{in}}{I_{in}} \simeq \frac{V_{in}}{V_{id}/R_i}$$

$$V_{id} \simeq \frac{V_o}{A} \quad \text{and} \quad V_o \simeq \frac{A}{1+AB} V_{in}$$



We have $R_{if} \simeq \frac{V_{in}}{} \simeq R_i V_{in}$

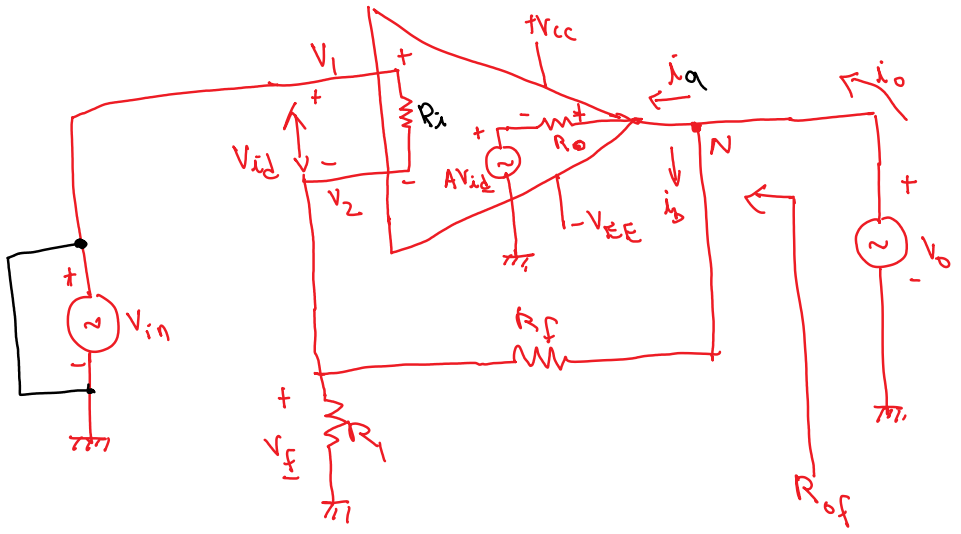
We have $R_{if} = \dfrac{V_{in}}{V_{id}/R_i} = \dfrac{R_i V_{in}}{V_{id}}$

$= \dfrac{R_i V_{in}}{V_o/A} = \dfrac{A R_i V_{in}}{V_o}$

$= \dfrac{A R_i V_{in}}{\frac{A}{1+AB} V_{in}}$

$$\boxed{R_{if} = R_i (1+AB)}$$

output resistance with feedback



Output resistance is the resistance determined looking back into the feedback amplifier from the output terminal. It is obtained by using Thevenin's theorem for dependant sources. To find output resistance with feedback, R_{of}, reduce the independant source V_{in} to zero, apply an external voltage V_o, then calculate the resulting current i_o.

$$R_{of} = \frac{V_o}{i_o}$$

At node N, Apply KCL

$$i_o = i_a + i_b$$

Since $(R_f + R_1) \| R_i \gg R_o$ and $i_a \gg i_b$

$$\therefore i_o \approx i_a \quad \hookrightarrow (1)$$

Apply KVL at o/p loop to obtain i_o

$$\text{ie, } V_o - R_o i_o - AV_{id} = 0$$

$$i_o = V_o - AV_{id}$$

$$\beta = \frac{V_f}{V_o}$$

$$V_f = \beta V_o$$

$$\frac{}{R_0}$$

$$\therefore I_0 = \frac{V_0 + AB V_0}{R_0}$$

$$\therefore (1) \Rightarrow R_{0f} = \frac{V_0}{\frac{V_0 + AB V_0}{R_0}} = \frac{R_0}{1+AB}$$

$$\boxed{R_{0f} = \frac{R_0}{1+AB}}$$

$$V_{id} = V_1 - V_2$$
$$= 0 - V_f$$
$$= 0 - \frac{R_1 V_0}{R_1 + R_f}$$
$$V_{id} = -BV_0$$

Bandwidth with feedback

Bandwidth of an amplifier is defined as the range of frequencies for which the gain remains constant.

Break frequency :- The frequency at which the gain A is 3dB down from its original value at 0Hz.

Unity Gain Bandwidth : The frequency at which gain equals 1

Since for an op-amp with a single break frequency f_0, the gain bandwidth product is constant and is equal to unity gain bandwidth

$$UGB = A f_0$$

A => open loop voltage gain
f_0 => break frequency of an op-amp

Alternatively

$$UGB = A_f f_F$$

A_f => closed loop voltage gain
f_F => bandwidth with feedback

$$\therefore A f_0 = A_f f_F$$

$$f_F = \frac{A f_0}{A_f}$$

for non-inverting amplifier $A_f = \frac{A}{1+AB}$

$$\therefore f_F = \frac{A f_0}{A/1+AB} = f_0(1+AB)$$

$$\boxed{f_F = f_0(1+AB)}$$

Total output offset voltage

Since with feedback, the gain of the non-inverting amplifier changes from A to $\frac{A}{1+AB}$, the total output offset voltage with feedback must also be $\frac{1}{1+AB}$ times the voltage without feedback

$$\text{Total offset voltage with feedback} = \frac{\text{total output offset voltage without feedback}}{1+AB}$$

$$V_{OOT} = \frac{\pm V_{sat}}{1+AB}$$

VOLTAGE SHUNT FEEDBACK AMPLIFIER

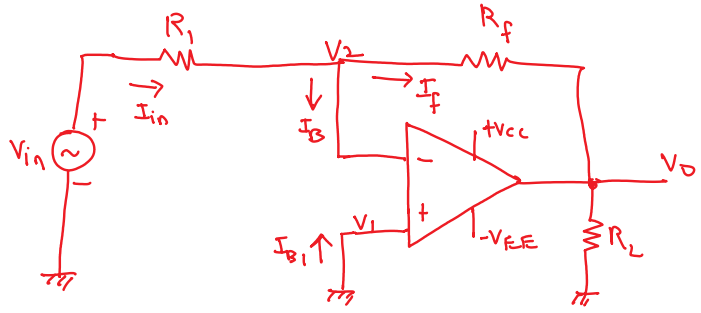


fig: Voltage shunt feedback amplifier (Inverting amplifier with feedback)

The input voltage drives the inverting terminal, and the amplified as well as inverted output signal is also fed back to the inverting input via feedback resistor R_f.

This forms a negative feedback because any increase in output signal results in a feedback signal into the inverting input, causing a decrease in the output signal.

Closed loop Voltage Gain

Apply KCL at node V_2

$$I_{in} = I_B + I_F$$

Since R_i is very large $I_B \approx 0$

$$\therefore \quad I_{in} = I_F$$

$$\frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_o}{R_f}$$

$\frac{V_o}{V_d} = A$

We have $V_1 - V_2 = \frac{V_o}{A}$

Since $V_1 = 0$ $\qquad V_2 = \frac{-V_o}{A}$

$$\therefore \quad \frac{V_{in} + \frac{V_o}{A}}{R_1} = \frac{-V_o/A - V_o}{R_f}$$

R_1 $\quad\quad$ R_F

$$V_{in} R_F + \frac{V_o}{A} R_F = -\frac{V_o}{A} R_1 - V_o R_1$$

$$V_o \left(\frac{R_F}{A} + \frac{R_1}{A} + R_1 \right) = -V_{in} R_F$$

$$V_o \left(R_F + R_1 + A R_1 \right) = -V_{in} A R_F$$

$$A_F = \frac{V_o}{V_{in}} = \frac{-A R_F}{R_F + R_1 + A R_1} \quad \text{(exact)}$$

The negative sign indicates the input and output are out of phase by 180°. Thus it is called Inverting amplifier

Since A is very large, $AR_1 >> R_f + R_1$

$$\therefore A_F = \frac{-A R_F}{A R_1}$$

$$A_f = \frac{-R_f}{R_1} \quad \text{(ideal)}$$

We have $A_f = \dfrac{-A R_F}{R_1 + R_F + A R_1}$

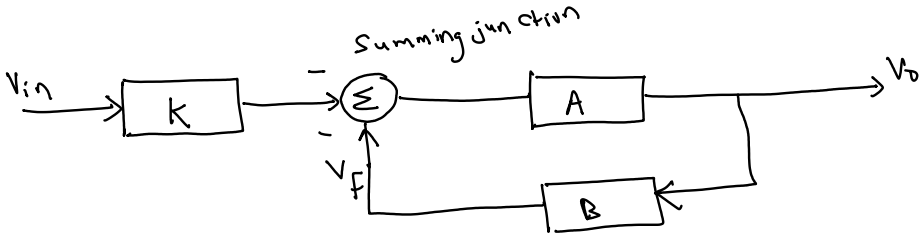
$$= \frac{\dfrac{-A R_F}{R_1 + R_F}}{\dfrac{R_1 + R_F}{R_1 + R_F} + \dfrac{A R_1}{R_1 + R_F}}$$

$$A_F = \frac{-AK}{1 + AB} \longrightarrow (1)$$

Where $K = \dfrac{R_F}{R_1 + R_F}$ a voltage attenuating factor

$$B = \frac{R_1}{R_1 + R_F}$$ Gain of feedback circuit

A comparison of gain of inverting amplifier (eqn ①) with gain of non inverting amplifier (Voltage series) is that the gain of inverting amplifier is k times that of non-inverting amplifier ($K < 1$) in addition to the phase inversion (− sign).



From eqn ① $$A_F = \frac{-KA}{1+AB}$$

If $AB >> 1$

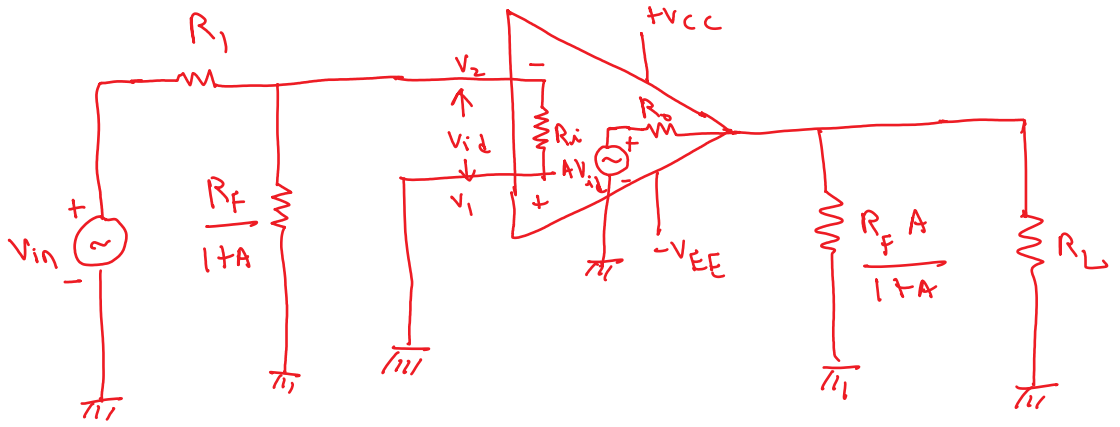
$1 + AB \approx AB$

$$A_f \approx \frac{-KA}{AB} = -\frac{k}{B}$$

$$= -\frac{R_F}{\frac{R_1 + R_F}{R_1}}$$

$$\therefore A_f = -\frac{R_F}{R_1}$$ (ideal case)

Input resistance with feedback



Inverting amplifier with millerized feedback resistor.

The easy method of finding the input resistance is to Millerize the feedback resistor R_F ie, split R_f in its Miller components

Input resistance with feedback

$$R_{iF} \simeq R_1 + \frac{R_F}{1+A} \,||\, R_i \qquad \text{exact}$$

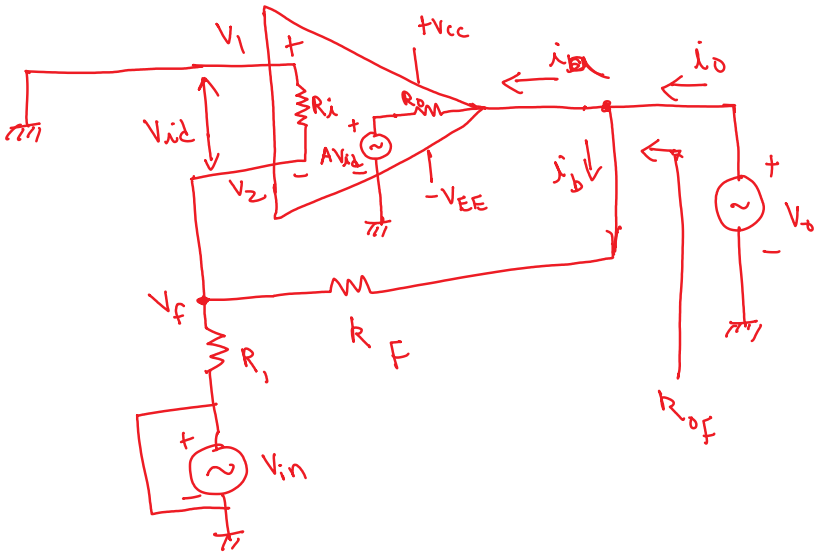
since R_i and A are large

$$\frac{R_F}{1+A} \,||\, R_i \approx 0$$

$$\therefore \quad R_{if} = R_1 \qquad (\text{Ideal})$$

Output resistance with feedback

The output resistance is the resistance measured at the output terminal of the feedback amplifier.



The output resistance is obtained by using Thevenin's theorem.

The output resistance is same as that of non inverting amplifier

$$\therefore R_{of} = \frac{R_o}{1+AB}$$

Bandwidth with feedback

The gain bandwidth product of a single break frequency op-amp is always constant.

The gain of the amplifier with feedback is always less than the gain without feedback.

Therefore, the bandwidth of the amplifier with feedback f_F must be larger than without feedback

$$f_F \simeq f_o (1 + AB) \quad \hookrightarrow (1)$$

where f_o = break frequency of the op-amp

$$= \frac{\text{unity gain bandwidth}}{\text{open-loop voltage gain}}$$

$$= \frac{UGB}{A}$$ (for single break frequency op-amp)

$$\therefore (1) \Rightarrow f_F \simeq \frac{UGB}{A}(1 + AB)$$

$$\simeq \frac{UGB\,(1 + AB)\,K}{AK}$$

$$\simeq \frac{UGB\,(K)}{A_F} \quad \hookrightarrow (2)$$

where $A_F \simeq \frac{AK}{1 + AB}$

and $K \simeq \frac{R_f}{R_1 + R_f}$

To find closed loop bandwidth use eqn (1) if f_o is given and use eqn (2) if UGB is given.

For same closed loop gain, the closed loop bandwidth of inverting amplifier is lower than non-inverting. by a factor of k $(k<1)$

.

Total output offset voltage with feedback

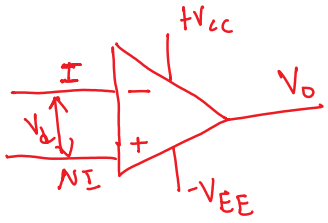
The gain of the op-amp with feedback is less than without feedback.

Therefore, the output offset voltage with feedback V_{OOT} must always be smaller than that without feedback.

$$\text{Total output offset voltage with feedback} = \frac{\text{total o/p voltage without feedback}}{1+AB}$$

$$V_{OOT} = \frac{\pm V_{sat}}{1+AB}$$ (same as inverting)

Virtual ground concept



$$A_{OL} = \frac{V_o}{V_{NI} - V_I} = \frac{V_o}{V_d}$$

For Ideal op-amp,

$A_{OL} = \infty$

Practical opamp (741)

$A_{OL} = 10^6$

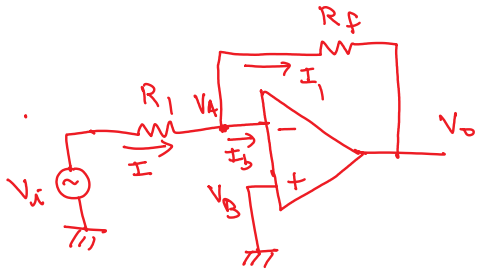
For ideal, $A_{OL} = \infty$

$$\frac{V_o}{V_d} = \infty$$

$$V_d \approx 0 \Rightarrow V_{NI} - V_I = 0$$

$$V_{NI} = V_I$$

Closed loop gain of ideal inverting op-amp



Since $V_B = 0$

By virtual ground Concept

$V_A = 0$

$I_b = 0$ (i/p resistance high)

At node A, apply KCL

$$I = I_b + I_1$$

$$I = I_1$$

$$\frac{V_i - V_A}{R_1} = \frac{V_A - V_o}{R_f}$$

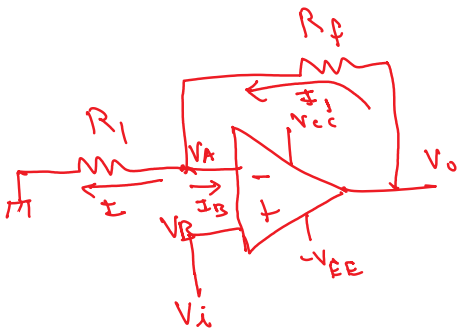
$$\frac{V_i - 0}{R_1} = \frac{0 - V_o}{R_f}$$

Ideal closed loop gain

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

-ve sign indicates i/p and o/p are 180° out of phase

Closed loop gain of ideal non- inverting op-amp



Here $V_B = V_i$

By virtual ground Concept

$V_A = V_B = V_i$

KCL at node A

$I_1 = I_B + I$

$I_1 = I$ ($I_B = 0$ i/p resistance is high)

$$\frac{V_o - V_A}{R_f} = \frac{V_A - 0}{R_1}$$

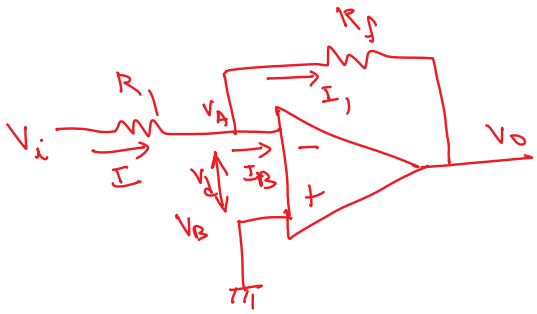
$$\frac{V_o - V_i}{R_f} = \frac{V_i}{R_1}$$

$$\frac{V_o}{R_f} = V_i\left(\frac{1}{R_1} + \frac{1}{R_f}\right)$$

$$\frac{V_o}{R_f} = V_i\left(\frac{R_f + R_1}{R_1 R_f}\right)$$

Ideal closed loop gain $A_{CL} = \frac{V_o}{V_i} = \frac{R_f + R_1}{R_1} = 1 + \frac{R_f}{R_1}$

Closed loop gain of practical inverting op-amp



Virtual ground concept is not applicable

$V_B = 0$

$V_A \neq V_B$

$V_d = V_B - V_A = -V_A$

Apply KCL at node A

$I = I_B + I_1$

$I = 0 + I_1$

$I = I_1$

$$\frac{V_i - V_A}{R_1} = \frac{V_A - V_o}{R_f}$$

For practical op-amp

$A_{OL} = \frac{V_o}{V_d}$

$A_{OL} = \frac{V_o}{-V_A}$

$V_A = \frac{-V_o}{A_{OL}}$

$$\frac{V_i + \frac{V_o}{A_{OL}}}{R_1} = \frac{\frac{-V_o}{A_{OL}} - V_o}{R_f}$$

$$V_i + \frac{V_o}{A_{OL}} = -\frac{R_1}{R_f} V_o \left(\frac{1}{A_{OL}} + 1\right)$$

$$V_o \left(\frac{1}{A_{OL}} + \frac{R_1}{R_f}\left(\frac{1}{A_{OL}} + 1\right)\right) = -V_i$$

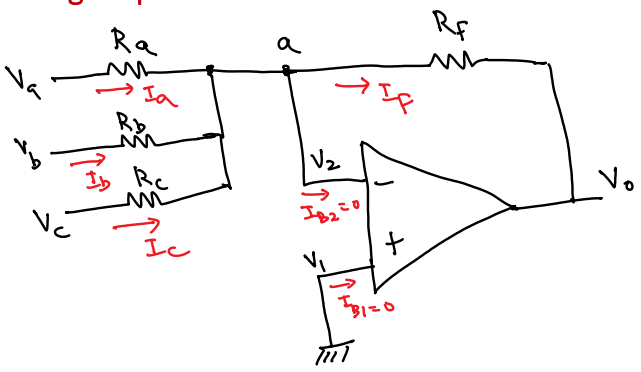
$$A_{CL} = \frac{V_o}{V_i} = \frac{-1}{\frac{1}{A_{OL}} + \frac{R_1}{R_f}\left(\frac{A_{OL}+1}{A_{OL}}\right)}$$

$$= \frac{-1}{\frac{R_f + R_1(1+A_{OL})}{A_{OL} R_f}}$$

Closed loop gain

$$A_{CL} = \frac{-A_{OL} R_f}{R_f + R_1 (1 + A_{OL})}$$

Summing Amplifier



At node a, apply KCL

$$I_a + I_b + I_c = I_f$$

$$\frac{V_a - 0}{R_a} + \frac{V_b - 0}{R_b} + \frac{V_c - 0}{R_c} = \frac{0 - V_o}{R_f}$$

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = -\frac{V_o}{R_f}$$

$$V_o = -\left(\frac{R_f}{R_a} V_a + \frac{R_f}{R_b} V_b + \frac{R_f}{R_c} V_c\right) \quad \hookrightarrow (1)$$

Case 1

Let $R_a = R_b = R_c = R$

$$V_o = -\frac{R_f}{R}\left(V_a + V_b + V_c\right)$$

Summing Amplified

Case 2

(1) $\Rightarrow$ scaling or weighted amplified

Case 3

Average circuit

If $R_a = R_b = R_c = R$

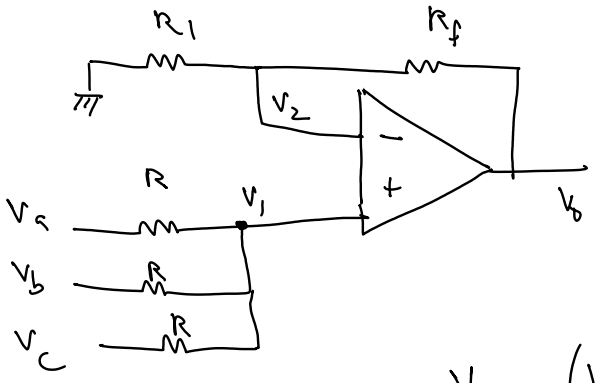
$$\frac{R_f}{R} = \frac{1}{n} \qquad n \Rightarrow \text{no. of i/ps}$$

$$V_o = -\frac{R_f}{R}\left(V_a + V_b + V_c\right)$$

$$= -\frac{1}{n}(V_a + V_b + V_c)$$

$n = 3$

$$V_o = -\frac{1}{3}(V_a + V_b + V_c)$$



summing amplifier in non-inverting mode

$\frac{R\,R}{R+R} = \frac{R}{2}$

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_1$$

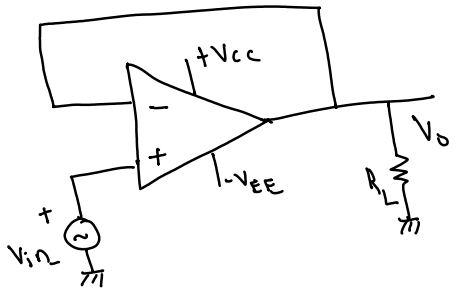
V_1 can be calculated using superposition theorem.

$$V_1 = V_a \frac{R/2}{R+R/2} + V_b \frac{R/2}{R+R/2} + V_c \frac{R/2}{R+R/2}$$

$$V_1 = \frac{V_a}{3} + \frac{V_b}{3} + \frac{V_c}{3}$$

$$\therefore V_o = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{V_a + V_b + V_c}{3}\right)$$

Voltage Follower



The lowest gain that can be obtained from a non-inverting amplifier with feedback is 1. When the non inverting amplifier is configured for unity gain, it is called voltage follower and the output is equal to and in phase with the input.

In voltage follower, output follows the input.

To obtain voltage follower from non-inverting amplifier, simply open R_1 and short R_F.

For voltage follower,

$$\Rightarrow A_F = 1$$

$$\Rightarrow R_{iF} = AR_i$$

$$\Rightarrow R_{oF} = \frac{R_o}{A}$$

$$\Rightarrow f_F = Af_o$$

$$\Rightarrow V_{oo_T} = \frac{\pm V_{sat}}{A}$$

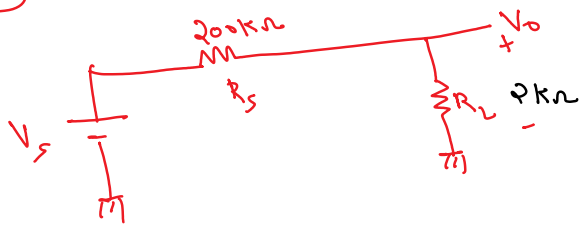
The voltage follower is also called a non-inverting buffer because when placed between two networks, it removes the loading on the first network.

⇒ It possess high input impedance and low output impedance

⇒ Since input impedence is high, whenever connected to source, it draws negligible current. Therefore source

is not loaded. This avoids loading effect.

Loading effect



$$V_o = V_s \frac{R_L}{R_s + R_L}$$

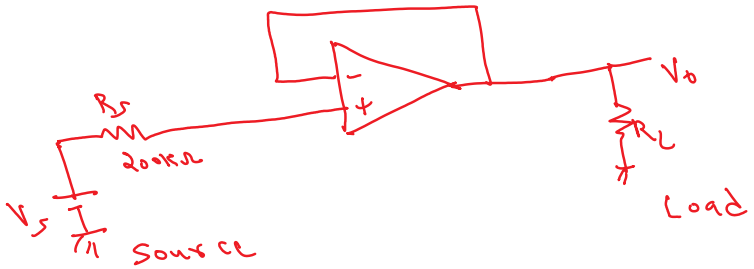
$$V_o = V_s \frac{2k\Omega}{(200+2)k\Omega} = 0.01 V_s$$

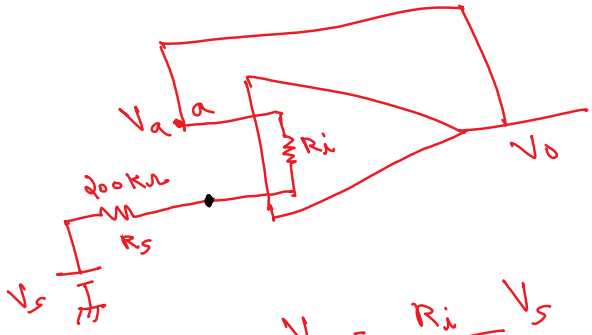
$$V_o = 0.01 V_s$$

Here source is severly attenuated.

Instead of V_s, o/p is measured as $\frac{V_s}{100}$ because of low input impedance

This attenuation is called loading effect.





$$V_a = \frac{R_i}{R_i + 200k\Omega} V_s$$

Since $R_i >> 200k\Omega$

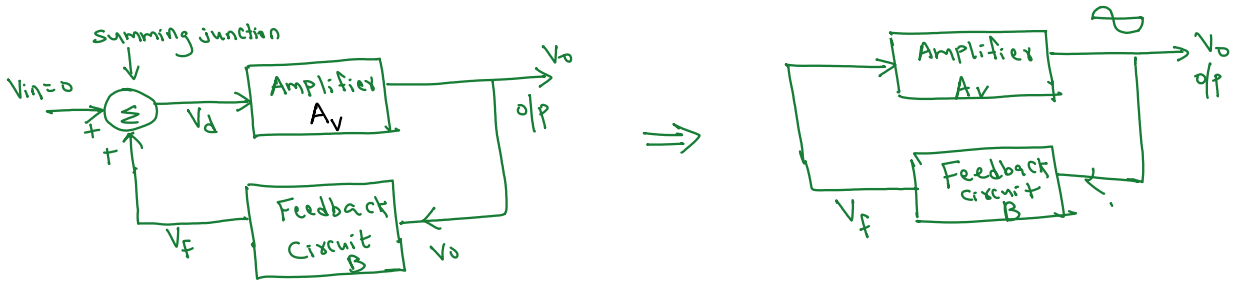
$$V_a \approx V_s$$

For voltage follower

$V_o = V_a = V_s$

OSCILLATORS

An oscillator is a type of feedback amplifier in which output is fed back to the input via a feedback circuit. If feedback is of proper magnitude and phase, circuit produces alternating currents or voltages.
Oscillators use positive feedback.



oscillator block diagram

From diagram,

$$V_d = V_f + V_{in}$$

$$V_o = A_v V_d$$

$$V_f = BV_o$$

$$V_o = A_V(V_f + V_{in})$$

$$V_o = A_V(BV_o + V_{in})$$

$$V_o = A_V BV_o + A_V V_{in}$$

$$V_o(1 - A_V B) = A_V V_{in}$$

$$\frac{V_o}{V_{in}} = \frac{A_V}{1 - A_V B}$$

$$A = \frac{A_V}{1 - A_V B}$$

If $V_{in} = 0 \Rightarrow 1 - A_V B = 0$

$\Rightarrow A_V B = 1$ for sustained oscillation

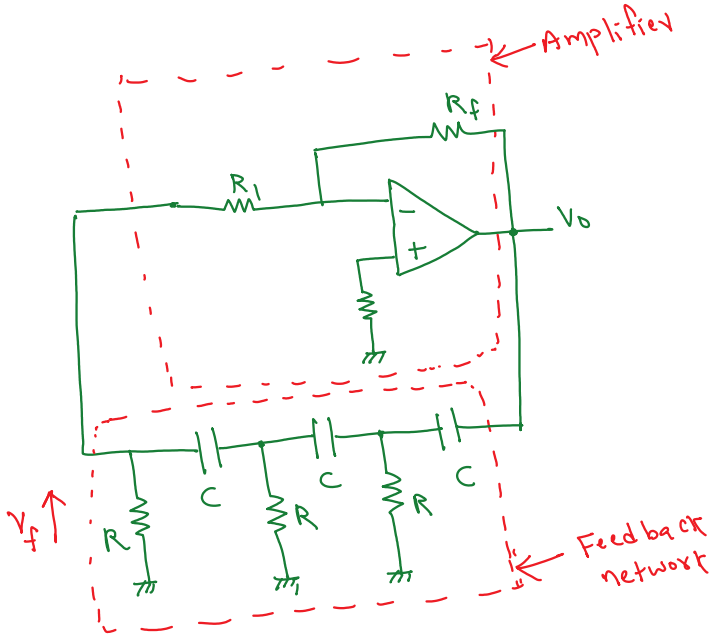
In polar form $A_V B = 1 \angle 0^\circ$ or 360°

Two conditions

1) $|A_V B| = 1$ (magnitude of loop gain $A_V B$ must be atleast 1)

2) Total phase shift must be 0° or 360°.

Phase shift Oscillator



RC phase shift oscillator consists of op-amp as the amplifying stage and three RC cascaded networks as the feedback circuit.

The op-amp is used in the inverting mode and it provides 180° phase shift.

Additional 180° phase shift is provided by 3 RC network stages (each 60°).

Thus the total phase shift is 360°

At some specific frequency, when the total phase shift of the cascaded RC networks is exactly 180° and the gain of the amplifier is sufficiently large, the circuit will oscillate at this frequency. This frequency is called the frequency of oscillation, f_o.

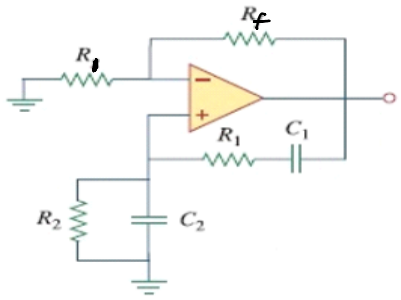
$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

At this frequency Gain must be atleast 29.

$$\left|\frac{R_f}{R_1}\right| = 29$$

$$R_f = 29R_1$$

Wein Bridge Oscillator



Most commonly used audio frequency oscillator.

Here a wein bridge circuit is connected between amplifier input terminal and the output terminal.

The bridge has a series RC network in one arm and a parallel RC network in the adjoining arm.

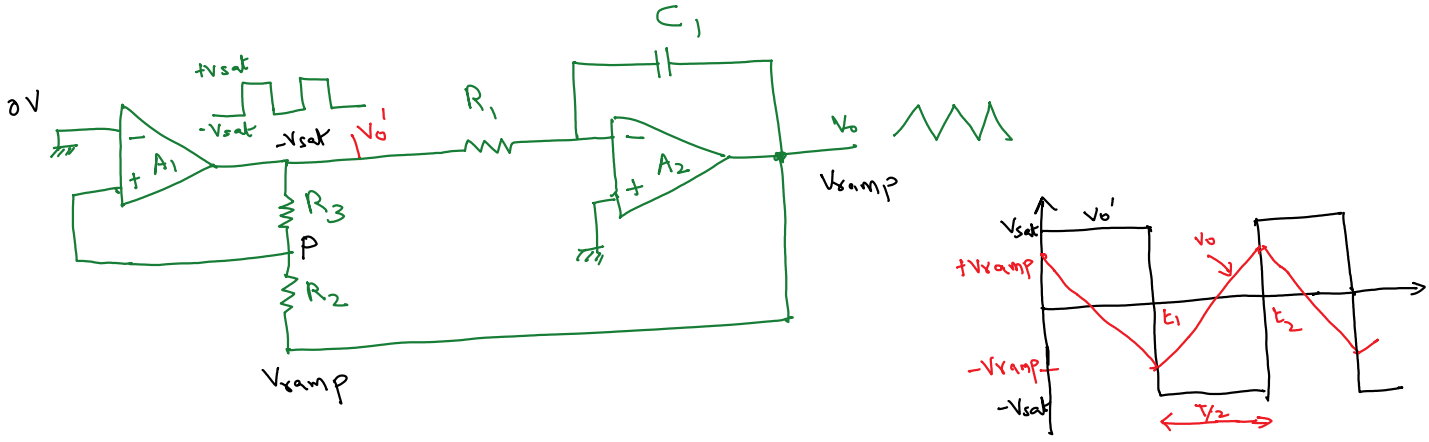
In the remaining two arms R_1 and R_f are connected.

The phase angle criterion for oscillation is that total phase shift is 0°. This condition occurs only when bridge is balanced, ie at resonance. the frequency of oscillation

$$f_o = \frac{1}{2\pi RC} = \frac{0.159}{RC}$$

$$\text{Gain } A_V = \frac{1}{B} = 3$$

Triangle waveform generator



A triangular wave can be obtained by integrating a square wave.
The output of comparator A1 is a square wave of amplitude ±Vsat and is applied to the negative input of the integrator A2 producing a triangular wave.
The triangular wave is fed back to the input to the comparator A1 through a voltage divider R2R3.

Let the output of the comparator is at +Vsat. The output of the integrator will be a negative going ramp.
Thus one end of the voltage divider R2R3is at a voltage +Vsat and other at the negative going ramp of A2.
At a time t=t1, when the negative going ramp attains a value of -Vramp, the effective voltage at P becomes slightly less than 0V. This switches the output of A1 from positive saturation to negative saturation level -Vsat.

During the time when the output of A1 is at -Vsat, the output of A2 increases in the positive direction.
At instant t=t2, the voltage at point P becomes just above 0V, thereby switching the output of A1 from -Vsat to + Vsat.
This cycle repeats and generates the triangular waveform.

The frequency of square and triangular waveforms remains same.
The amplitude of the triangular wave depends on the RC value of integrator A2 and the output level of A1.

The effective voltage at point P during the time when o/p of A_1 is at $+V_{sat}$

$$V_p = -V_{ramp} + (V_{sat} - (-V_{ramp}))\frac{R_2}{R_2+R_3}$$

At $t = t_1$, the voltage at P becomes equal to zero

i.e, $V_p = 0$

$$\Rightarrow 0 = -V_{ramp} + (V_{sat} + V_{ramp})\frac{R_2}{R_2+R_3}$$

$$= -V_{ramp} + V_{sat}\frac{R_2}{R_2+R_3} + V_{ramp}\frac{R_2}{R_2+R_3}$$

$$-V_{sat}\frac{R_2}{R_2+R_3} = V_{ramp}\left(\frac{R_2}{R_2+R_3} - 1\right)$$

$$-V_{sat}\frac{R_2}{R_2+R_3} = V_{ramp}\left(\frac{R_2 - R_2 - R_3}{R_2+R_3}\right)$$

$$-V_{sat}\frac{R_2}{R_2+R_3} = V_{ramp}\left(\frac{R_2 - R_2 - R_3}{R_2+R_3}\right)$$

$$-V_{sat}R_2 = -V_{ramp}R_3$$

$$-V_{ramp} = -\frac{R_2}{R_3}V_{sat} \quad \hookrightarrow (1)$$

(iii) at $t = t_2$, when the o/p of A_1 switches from $+V_{sat}$ to $-V_{sat}$

$$(1) \Rightarrow V_{ramp} = -\frac{R_2}{R_3}(-V_{sat})$$

$$= \frac{R_2}{R_3}V_{sat} \quad \hookrightarrow (2)$$

Peak to peak amplitude of triangular wave

$$V_o(pp) = +V_{ramp} - (-V_{ramp})$$

$$= \frac{R_2}{R_3}V_{sat} - \left(-\frac{R_2}{R_3}V_{sat}\right)$$

$$\hookrightarrow (3)$$

$$V_{o(pp)} = 2\frac{R_2}{R_3}V_{sat}$$

o/p of Integrator

$$V_o = -\frac{1}{RC}\int V_i\,dt$$

$\therefore$ o/p switches from $-V_{ramp}$ to V_{ramp} in $T/2$ seconds

$$\therefore V_{o(pp)} = -\frac{1}{R_1C_1}\int_0^{T/2}(-V_{sat})\,dt$$

$$= \frac{V_{sat}}{R_1C_1}(t)_0^{T/2}$$

$$V_{o(pp)} = \frac{V_{sat}}{R_1C_1}\left(\frac{T}{2}\right)$$

$$2\frac{R_2}{R_3}V_{sat} = V_{sat}\left(\frac{T}{2}\right) \quad (\text{from eqn } (3))$$

$$\frac{2R_2}{R_3}V_{sat} = \frac{V_{sat}}{R_1 C_1}\left(\frac{T}{2}\right)$$

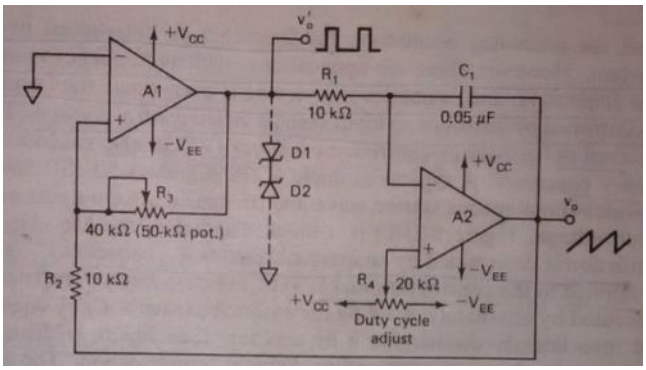
(from eqn (3))

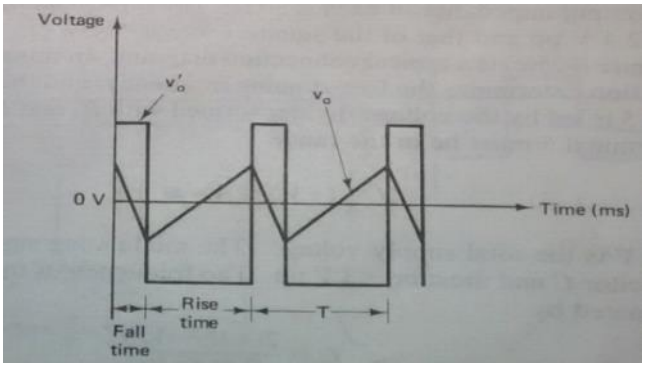
$$T = \frac{4R_1 C_1 R_2}{R_3}$$

∴ frequency of oscillation

$$f = \frac{1}{T} = \frac{R_3}{4R_1 C_1 R_2}$$

Sawtooth wave generator





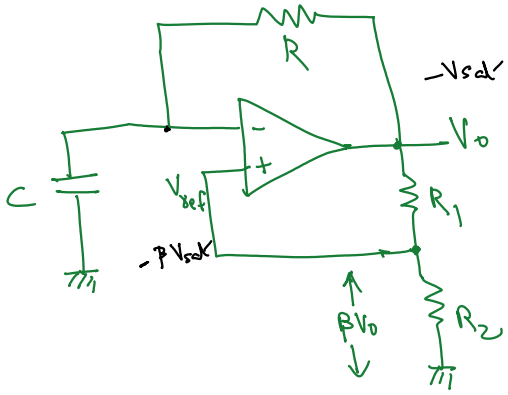
The difference between the triangular wave and sawtooth waveform is that the rise time of triangular wave is always equal to its fall of time while in saw tooth generator, rise time may be much higher than its fall of time , vice versa.

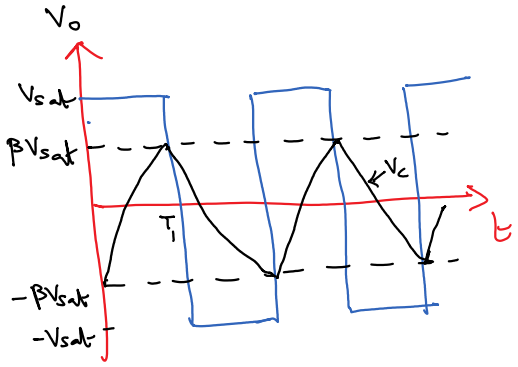
The triangular wave generator can be converted in to a sawtooth wave generator by injecting a variable dc voltage into the non-inverting terminal of the integrator.

In this circuit a potentiometer is used. Now the output of integrator is a triangular wave riding on some dc level that is a function of R4 setting. The duty cycle of square wave will be determined by the polarity and amplitude of dc level.
A duty cycle less than 50% will cause output of integrator be a sawtooth. With the wiper at the centre of R4, the output of integrator is TRIANGULAR wave.
Use of the potentiometer is when the wiper moves towards −VEE, the rise time of the sawtooth become longer than the fall time. If the wiper moves towards +VCC , the fall time becomes more than the rise time.

Astable Multivibrator

→ Also called free running oscillator. Quasi stable





A fraction $\beta = \frac{R_2}{R_1+R_2}$ is fed back to the (+) input.

The reference voltage V_{ref} is βV_o which takes values $+\beta V_{sat}$ or $-\beta V_{sat}$.

The o/p is also fedback to the (-) input through a lowpass RC network.

Whenever input at the (-) input exceeds V_{ref}, switching takes place resulting in a square wave input.

When o/p is at $+V_{sat}$, the capacitor starts charging towards $+V_{sat}$ through R. The voltage at (+) input is at $+\beta V_{sat}$. This condition continues as the charge on C rises, until it just exceeded $+\beta V_{sat}$, the reference voltage.

When the voltage at (-) input terminal becomes just greater than the this reference voltage, the output is driven to $-V_{sat}$. At this instant the voltage on capacitor is $+\beta V_{sat}$. It begins to discharge through R, that is, charges towards $-V_{sat}$.

When the output switches to $-V_{sat}$, the capacitor charges more and more negatively until its voltage exceeds $-\beta V_{sat}$. The output switches back to $+V_{sat}$. The cycle repeats.

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa.

The voltage across capacitor $-t/RC$

The Voltage across Capacitor

$$V_c(t) = V_f + (V_i - V_f)\, e^{-t/RC}$$

final value $V_f = +V_{sat}$

Initial value $V_i = -\beta V_{sat}$

$$\therefore V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

$$V_c(t) = V_{sat} - V_{sat}(\beta+1)\, e^{-t/RC} \quad \longrightarrow (1)$$

At $t = T_1$, the Voltage across Capacitor reaches βV_{sat} and switching takes place

$$(1) \Rightarrow \quad V_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}(\beta+1)\, e^{-T_1/RC}$$

$$\beta = 1 - (\beta+1)\, e^{-T_1/RC}$$

$$(\beta+1)\, e^{-T_1/RC} = 1-\beta$$

$$e^{-T_1/RC} = \frac{1-\beta}{1+\beta}$$

$$-\frac{T_1}{RC} = \ln\left(\frac{1-\beta}{1+\beta}\right)$$

$$T_1 = -RC \ln\left(\frac{1-\beta}{1+\beta}\right)$$

$$T_1 = RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

Total time period

$$T = 2T_1 = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$\beta = \frac{R_2}{R_1+R_2}$$

If $R_1 = R_2$ then $\beta = 0.5$

$$T = 2RC \ln 3$$

If $R_1 = 1.16\, R_2$

$$T = 2RC$$

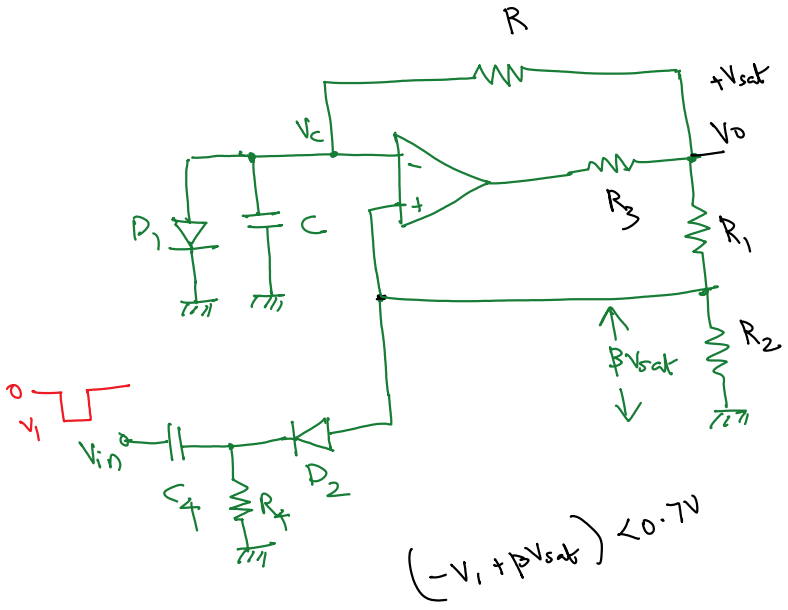
$$f_0 = \frac{1}{2RC}$$

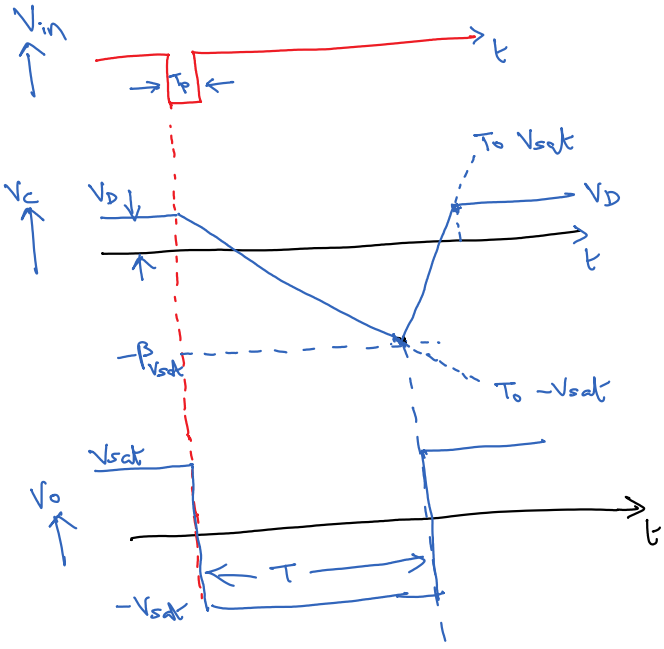
The o/p swings from $+V_{sat}$ to $-V_{sat}$

$$\therefore V_o(pp) = V_{sat} - -V_{sat}$$
$$= 2V_{sat}$$

Monostable Multivibrator

It has one stable stable and other is quasi stable state.





A diode D_1 clamps the capacitor voltage to 0.7 V when the output is at $+V_{sat}$. A negative going pulse signal of magnitude V_1 passing through the differentiator R_4 C_4 and diode D_2 produces a negative going trigger impulse and is applied to (+) input.

Let us assume that in stable stable, the output is at $+V_{sat}$. The diode D_1 conducts and V_c the voltage across capacitor gets clamped to 0.7 V.

The voltage at (+) input terminal through $R_1 R_2$ divider is $+\beta V_{sat}$. Now if a negative trigger of magnitude V_1 is applied to the (+) input terminal so that the effective signal at this terminal ie; $[\beta V_{sat} + (-V_1) < 0.7V]$, the o/p will switch from $+V_{sat}$ to $-V_{sat}$. The diode will now get reverse biased and the capacitor starts charging exponentially to $-V_{sat}$ through the resistance R. The voltage at (+) input terminal is now $-\beta V_{sat}$.

When capacitor voltage V_c becomes just slightly more negative

than $-\beta V_{sat}$, the o/p of the op-amp switches back to $+V_{sat}$. The capacitor C now starts charging to $+V_{sat}$ through R until V_c is 0.7V.

$$V_c = V_f + (V_i - V_f)\, e^{-t/RC}$$

$$V_c = -V_{sat} + (V_D + V_{sat})\, e^{-t/RC} \quad \hookrightarrow (1)$$

$V_f = -V_{sat}$

$V_i = V_D$

at $t = T$, $V_c = -\beta V_{sat}$

$$(1) \Rightarrow -\beta V_{sat} = -V_{sat} + (V_D + V_{sat})\, e^{-T/RC}$$

$$(1-\beta) V_{sat} = (V_D + V_{sat})\, e^{-T/RC}$$

$$(1-\beta) = \left(\frac{V_D + V_{sat}}{V_{sat}}\right) e^{-T/RC}$$

$$(1-\beta) = \left(1 + V_D/V_{sat}\right) e^{-T/RC}$$

$$e^{-T/RC} = \frac{1-\beta}{1 + V_D/V_{sat}}$$

$$-T/RC = \ln\left(\frac{1-\beta}{1 + V_D/V_{sat}}\right)$$

$$T = -RC \ln\left(\frac{1-\beta}{1 + V_D/V_{sat}}\right)$$

$$= RC \ln\left(\frac{1 + V_D/V_{sat}}{1-\beta}\right)$$

where $\beta = \frac{R_2}{R_1 + R_2}$

If $V_{sat} \gg V_D$ and $R_1 = R_2$ $\beta = 0.5$

then $\boxed{T = 0.69RC}$

$T_p \ll T$

Active filters : Comparison with passive filters

An electric filter is a frequency selective circuit that passes a specified band of frequencies and blocks signals of frequencies outside this band.
Active filters are the electronic circuits, which consist of active element like transistors op-amp(s) along with passive elements like resistor(s) and capacitor(s).

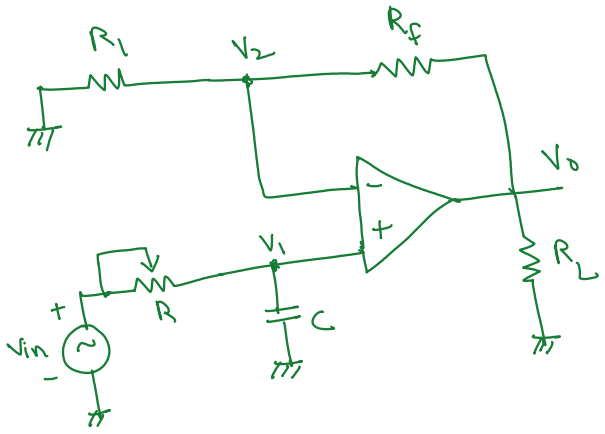
Elements used in passive filters are resistors, capacitors and inductors.

An active filter offers the following advantages over a passive filter.

1. Gain and frequency adjustment flexibility. Since the op-amp is capable of providing a gain, the input signal is not attenuated as it is in a passive filter. Also, the active filter is easier to tune or adjust.
2. No loading problem. Because of high input impedance and low output impedance of op-amp, the active filter does not cause loading of the source or load.
3. Cost. Active filters are more economical than passive filters.

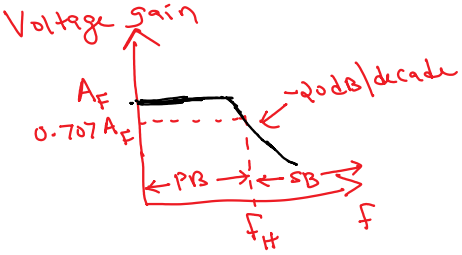
The most commonly used filters are
1. Low pass filter
2. High pass filter
3. Band pass filter
4. Band reject filter
5. All pass filter

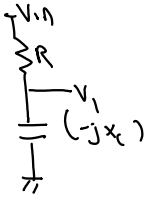
First order low-pass filter



op-amp is used in the non-inverting mode.

Resistors R_1 and R_f determine the gain of the filter.





$$V_1 = V_{in}\frac{(-jX_c)}{R - jX_c}$$

$$= V_{in}\frac{\left(\frac{1}{j2\pi fC}\right)}{R + \frac{1}{j2\pi fC}}$$

$$V_1 = V_{in}\left(\frac{1}{1 + j2\pi fRC}\right)$$

$$V_o = \left(1 + \frac{R_f}{R_1}\right)V_1$$

$$= \left(1 + \frac{R_f}{R_1}\right)\frac{V_{in}}{1 + j2\pi fRC}$$

$$\frac{V_o}{V_{in}} = \frac{1 + \frac{R_f}{R_1}}{1 + j2\pi fRC} = \frac{A_f}{1 + j(f/f_H)}$$

where $A_f = 1 + \frac{R_f}{R_1}$ passband gain

$f_H = \frac{1}{2\pi RC}$ higher cutoff frequency

$f \rightarrow$ i/p signal frequency

$$\frac{V_o}{V_{in}} = \frac{A_f}{1 + jf/f_H}$$

$a + jb$

$\sqrt{a^2 + b^2}$

$\tan^{-1} b/a$

Magnitude $\left|\frac{V_o}{V_{in}}\right| = \frac{A_f}{\sqrt{1+\left(f/f_H\right)^2}}$

Phase $\phi = 0 - \tan^{-1} f/f_H$

$= -\tan^{-1} f/f_H$

Case 1 $f < f_H$ $\left|\frac{V_o}{V_{in}}\right| = A_F$

Case 2 $f = f_H$ $\left|\frac{V_o}{V_{in}}\right| \simeq \frac{A_F}{\sqrt{2}} = 0.707\, A_f$

Case 3 $f > f_H$ $\left|\frac{V_o}{V_{in}}\right| < A_f$

Filter design

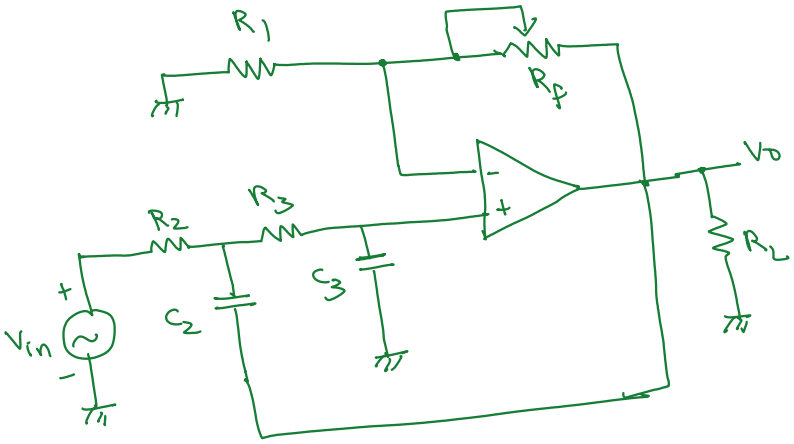
1. choose a value of high cut-off frequency f_H
2. select C less than or equal to 1MF.
3. calculate R

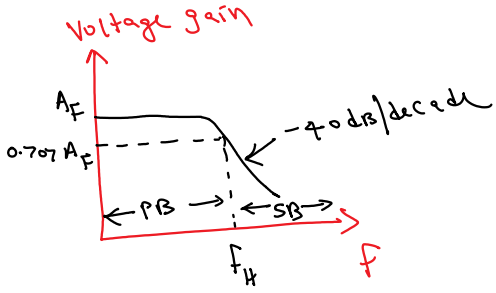
$f_H = \frac{1}{2\pi RC}$

$R = \frac{1}{2\pi f_H C}$

4) $A_F = 1 + \frac{R_f}{R_1}$ select R_1 and R_f

Second-order lowpass Filter





A stob band response having a 40dB/decade roll-off is obtained with second order lowpass filter.

A first order filter can be converted to second order filter by using an additional RC network.

The gain of the second order filter is set by R_1 and R_f while the gain of high cutoff frequency f_H is determined by R_2, C_2, R_3, C_3

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(f/f_H)^4}}$$

$$A_F = 1 + \frac{R_f}{R_1}$$ passband gain

Filter design

1) choose a value for f_H.
2) set $R_2 = R_3 = R$ and $C_2 = C_3 = C$

   Choose $C \leq 1\mu F$

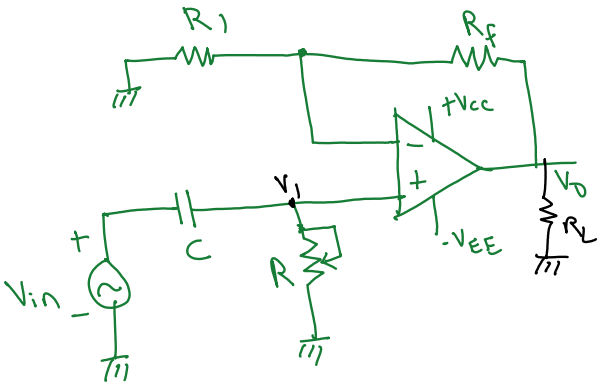
3) $R = \frac{1}{2\pi f_H C}$

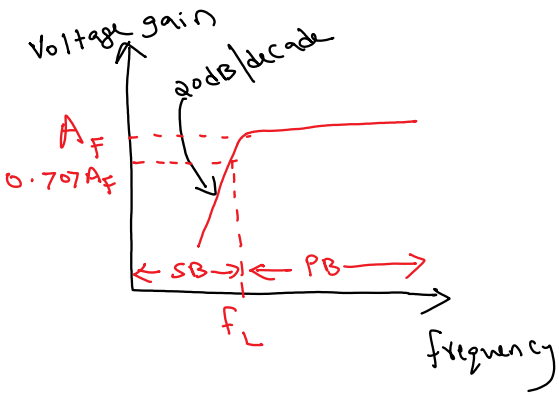
4) passband gain $A_f = 1 + \frac{R_f}{R_1} = 1.586$

$\therefore R_f = 0.586 R_1$

Choose $R_1 \leq 100k\Omega$ and calculate R_f

First order High pass filter





First order high pass filter is obtained by interchanging R and C in first order lowpass filter.

f_L is the low cutoff frequency.

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_1$$

$$V_o = \left(1 + \frac{R_f}{R_1}\right) \frac{j2\pi fRC}{1 + j2\pi fRC} V_{in}$$

$$\frac{V_o}{V_{in}} = A_f \frac{j\left(\frac{f}{f_L}\right)}{1 + j\frac{f}{f_L}} \quad \hookrightarrow (1)$$

where $A_f = 1 + \frac{R_f}{R_1}$ ← pass band gain

$f_L = \frac{1}{2\pi RC}$

f_L = low cutoff frequency

$$V_1 = V_{in} \frac{R}{R - jX_C}$$

$$= V_{in} \frac{R}{R - \frac{j}{2\pi fC}}$$

$$= V_{in} \frac{2\pi fRC}{2\pi fRC - j}$$

$$= V_{in} \frac{j2\pi fRC}{j2\pi fRC - j^2}$$

$$= V_{in} \frac{j2\pi fRC}{1 + j2\pi fRC}$$

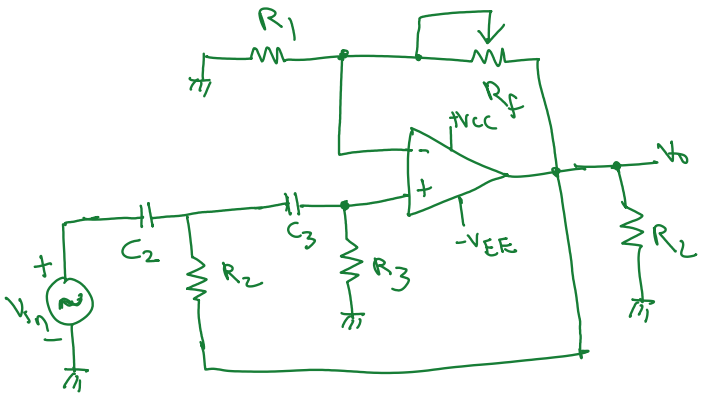
magnitude of voltage gain

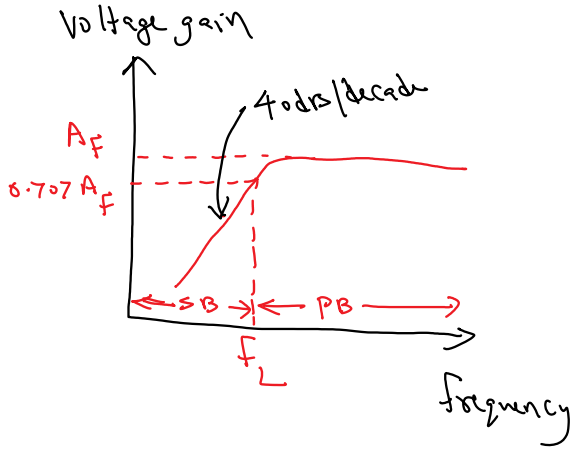
$$(1) \Rightarrow \left|\frac{V_o}{V_{in}}\right| = \frac{A_f \left(f/f_L\right)}{\sqrt{1 + (f/f_L)^2}}$$

$\frac{a+jb}{\sqrt{a^2+b^2}}$

$$= \frac{A_f}{\sqrt{\left(\frac{f_L}{f}\right)^2 + \left(\frac{f}{f_L}\right)^2 \left(\frac{f_L}{f}\right)^2}} \qquad = \frac{A_f}{\sqrt{1 + \left(\frac{f_L}{f}\right)^2}}$$

Second order High pass filter





A second order high pass filter can be formed from a second order lowpass filter by simply interchanging R and C.

Voltage gain magnitude $\left|\frac{V_o}{V_{in}}\right| = \frac{A_f}{\sqrt{1+\left(f_L/f\right)^4}}$

Band-pass Filter

A bandpass filter has a passband between two cutoff frequencies f_H and f_L such that $f_H > f_L$
Any input frequencies outside this passband is attenuated.

Two types
1. Wide bandpass $Q < 10$
2. Narrow bandpass $Q > 10$

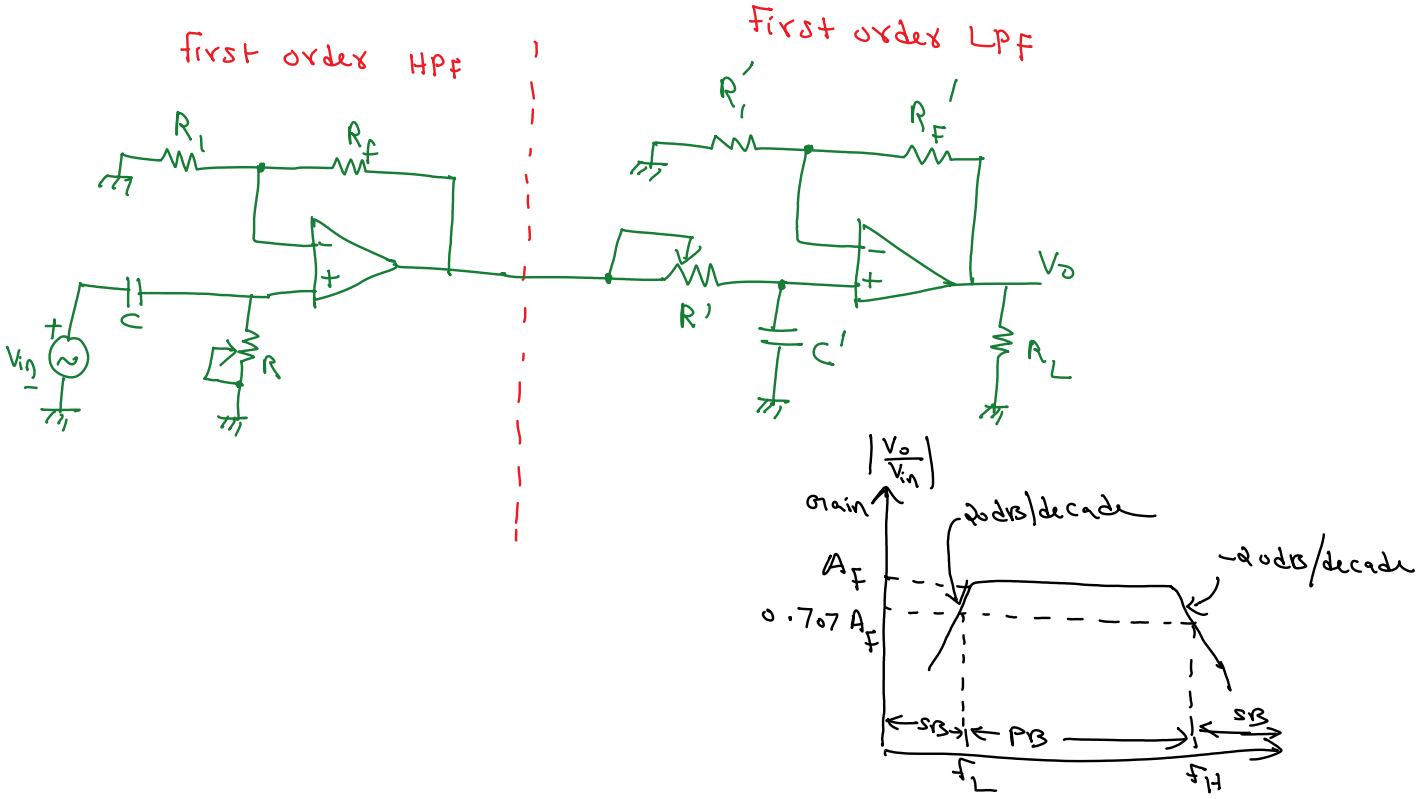
Q is a measure of selectivity, higher the value of Q, the more selective is the filter or narrower its bandwidth.

$$Q = \frac{f_c}{BW} = \frac{f_c}{f_H - f_L}$$

For wide band pass filter, center frequency $f_c = \sqrt{f_H f_L}$

For narrow bandpass filter, the output peaks at f_c.

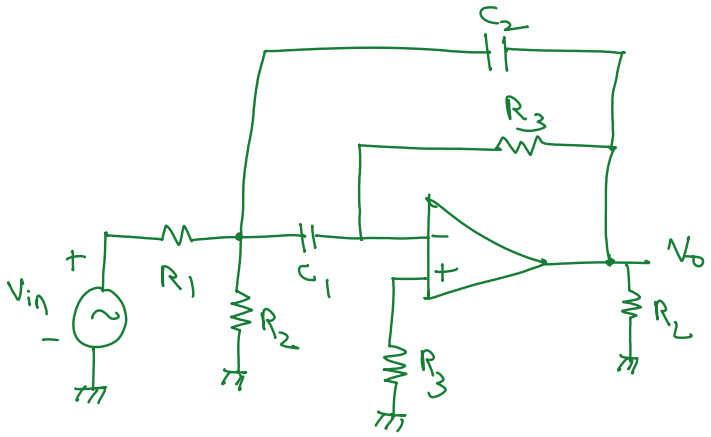
Wide band-pass Filter



A wide bandpass filter can be obtained by cascading a first order HPF with a first order LPF.

Narrow band-pass Filter

1. Multiple feedback filter since it has two feedback paths
2. The op-amp is used in the inverting mode.



Choose $C_1 = C_2 = C$

$$R_1 = \frac{Q}{2\pi f_c C A_F} \qquad R_2 = \frac{Q}{2\pi f_c C (2Q^2 - A_F)}$$

$$R_3 = \frac{Q}{\pi f_c C}$$

A_f is the gain at f_c $\qquad A_F = \frac{R_3}{2R_1}$

Gain $A_f < 2Q^2$

Advantage of multi feedback filter is that the center frequency f_c can be changed to a new frequency f_c' without changing gain or bandwidth. This is done by changing R_2 to R_2'

$$R_2' = R_2 \left(\frac{f_c}{f_c'}\right)^2$$

Band Reject Filter

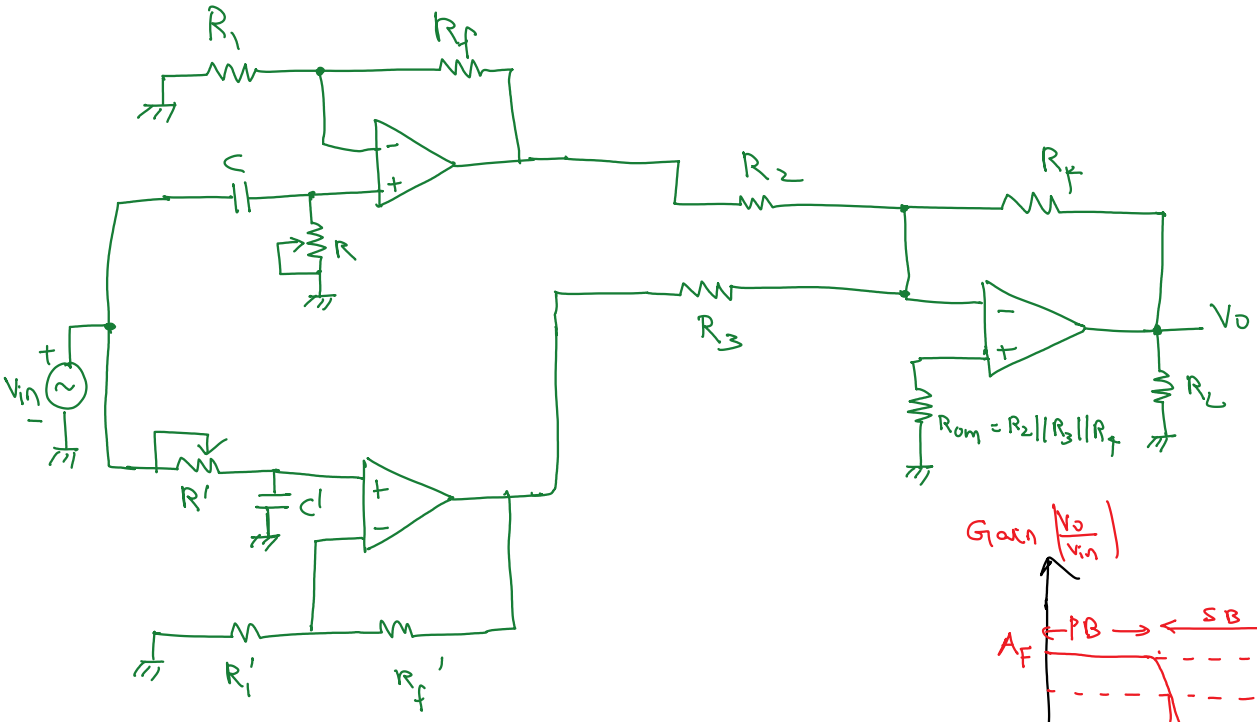
Also known as Band stop or Band elimination filter

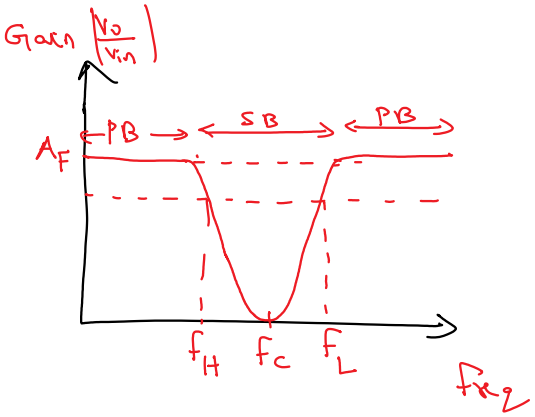
Here frequencies are attenuated in the stopband while they are passed outside this band.

Two types

1. Wide band reject
2. Narrow band reject

Wide band reject Filter





It consists of a LPF, HPF and a summing amplifier.
The low cutoff frequency of the HPF f_L must be larger than the high cutoff f_H frequency of the LPF.
The pass band gain of both high pass and low pass section must be equal.

Narrow band reject filter

Also known as notch filter.
Used for rejection of a single frequency such as 60-Hz power line frequency hum.
Commonly used notch filter is twin-T network. This is a passive filter composed of two T-shaped networks. One T network is made up of two resistors and a capacitor, while the other uses two capacitors and a resistor.
The notch-out frequency is the frequency at which maximum attenuation occurs.

$$f_N = \frac{1}{2\pi RC}$$

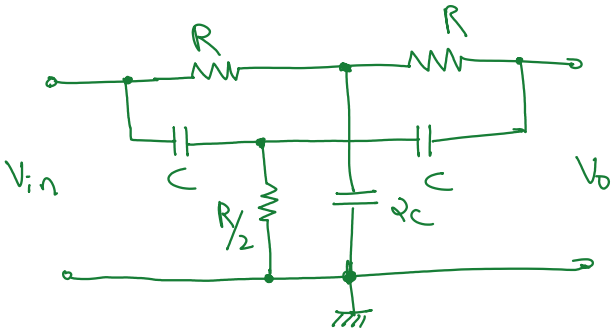
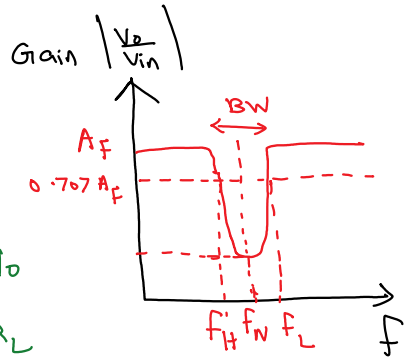
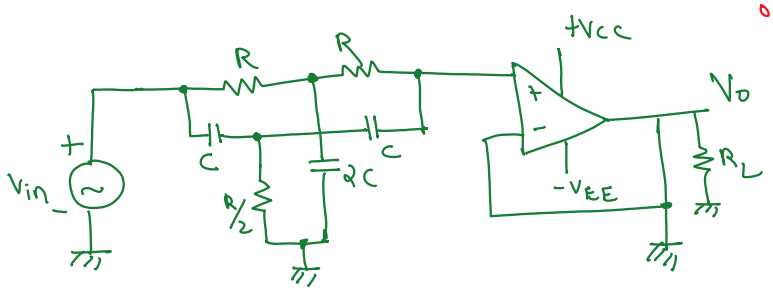


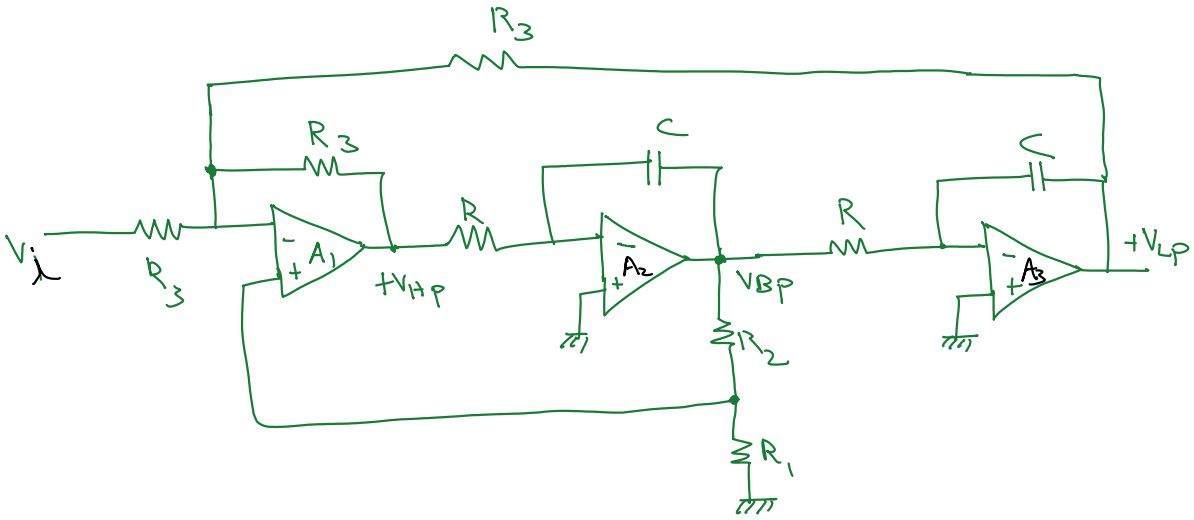
fig : Twin-T Network





The passive twin-T network has low figure of merit Q.
The Q of the network can be increased if it is used with the voltage follower.

State variable filter



The state variable filter uses two op-amp integrators and one op-amp adder to provide simultaneous second order lowpass, band pass and high pass filter responses.

o/p of op-amp A_2

$$V_{BP} = -\frac{1}{RCs} V_{HP}$$

$$V_o = -\frac{1}{RC}\int V_i\, dt$$

$$V_o(s) = \frac{-1}{RC}\frac{V_i(s)}{s}$$

$R = 1M\Omega \quad C = 1\mu F$

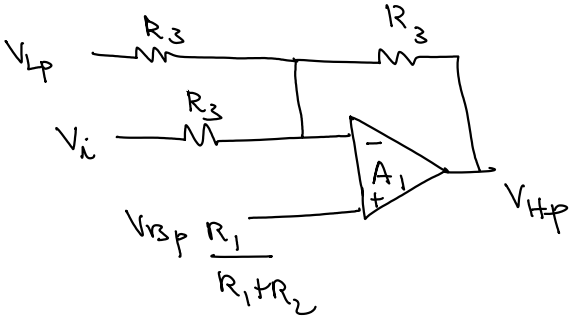
$$V_{BP} = -\frac{1}{s} V_{HP} \longrightarrow (1)$$

o/p of op-amp A_3

$$V_{LP} = -\frac{1}{s} V_{BP}$$

$$= -\frac{1}{s}\left(-\frac{1}{s} V_{HP}\right) = \frac{1}{s^2} V_{HP} \longrightarrow (2)$$

By superposition theorem



$$V_{HP} = -\frac{R_3}{R_3} V_i - \frac{R_3}{R_3} V_{LP} + \left(1 + \frac{R_3}{R_3 \| R_3}\right) V_{BP} \frac{R_1}{R_1+R_2}$$

$$= -V_i - V_{LP} + 3 V_{BP} R_1$$

$\frac{R_3}{R_3}$

$$= -V_i - V_{Lp} + 3 V_{Bp} \frac{R_1}{R_1 + R_2}$$

$\frac{R_3 R_3}{R_3 + R_3}$

$$V_{Hp} = -V_i - V_{Lp} + \alpha V_{Bp} \longrightarrow (3)$$

Damping factor $\alpha = 3 \frac{R_1}{R_1 + R_2}$

HPF

Substituting (1) and (2) in (3)

$$V_{Hp} = -V_i - \frac{1}{s^2} V_{Hp} + \alpha \left(-\frac{1}{s} V_{Hp} \right)$$

$$V_{Hp} \left(1 + \frac{1}{s^2} + \frac{\alpha}{s} \right) = -V_i$$

$$V_{Hp} \left(s^2 + \alpha s + 1 \right) = -V_i s^2$$

Highpass transfer function $H_{Hp} = \frac{V_{Hp}}{V_i} = \frac{-s^2}{s^2 + \alpha s + 1}$

Comparing with standard high pass transfer function

$$\frac{A_0 s^2}{s^2 + \alpha w_1 s + w_1^2}$$

$A_0 = -1$ and $w_1 = 1$

LPF

from (2) $\Rightarrow$ $V_{Hp} = s^2 V_{Lp}$

(1) $\Rightarrow$ $V_{Bp} = -\frac{1}{s} V_{Hp}$

$$= -\frac{1}{s} (s^2 V_{Lp}) = -s V_{Lp}$$

$\therefore$ substituting in (3)

(3) $\Rightarrow$

$$s^2 V_{Lp} = -V_i - V_{Lp} - \alpha s V_{Lp}$$

$$V_{Lp}(s^2 + \alpha s + 1) = -V_i$$

Lowpass transfer function $H_{Lp} = \frac{V_{Lp}}{V_i} = \frac{-1}{s^2 + \alpha s + 1}$

on Comparing

$$A_0 = -1 \qquad \omega_1 = 1$$

BPF

$$V_{Bp} = -\frac{1}{s} V_{Hp}$$

$$V_{Hp} = -s V_{Bp}$$

$$V_{Lp} = \frac{1}{s^2} V_{Hp}$$

$$= \frac{1}{s^2}(-s V_{Bp})$$

$$V_{Lp} = -\frac{1}{s} V_{Bp}$$

(3) $\Rightarrow$ $$-s V_{Bp} = -V_i + \frac{1}{s} V_{Bp} + \alpha V_{Bp}$$

$$V_{Bp}\left(s + \frac{1}{s} + \alpha\right) = V_i$$

$$V_{Bp}(s^2 + \alpha s + 1) = s V_i$$

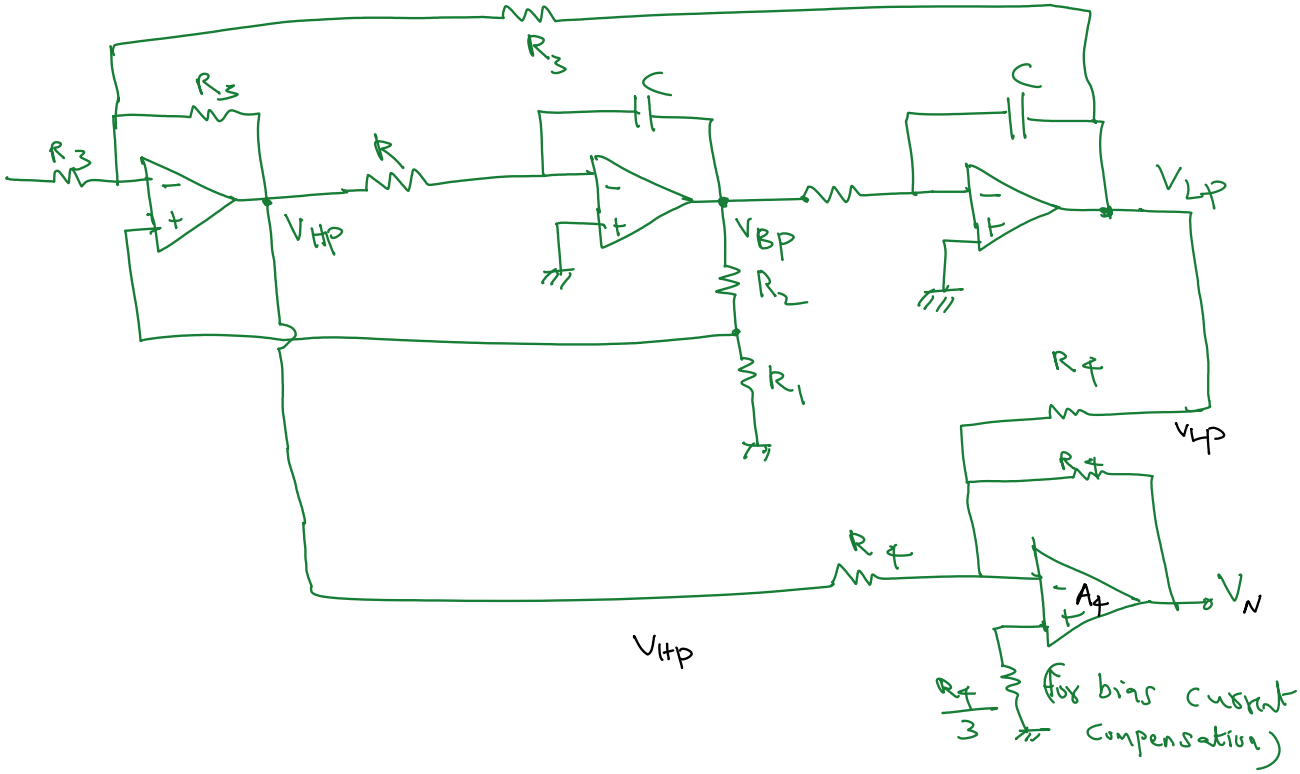
Band pass transfer function $H_{Bp} = \frac{V_{Bp}}{V_i} = \frac{s}{s^2 + \alpha s + 1}$

Comparing with general eqn

$$\frac{A_0 \alpha \omega_0 s}{s^2 + \alpha \omega_0 s + \omega_0^2}$$

$$A_0 \alpha \omega_0 = 1$$

$$\omega_0 = 1 = \frac{1}{RC}$$



The circuit modified to get a notch filter response

The op-amp A_f provides the notch filter response by combining LPF and HPF o/p

$$V_N = -\frac{R_f}{R_f} V_{Hp} - \frac{R_f}{R_f} V_{Lp}$$

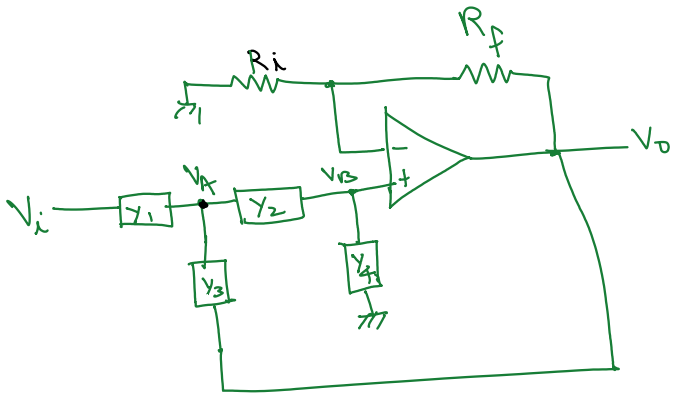
$$= -V_{Hp} - V_{Lp}.$$

$$V_N = -\left(\frac{-s^2}{s^2+\alpha s+1}\right)V_i - \left(\frac{-1}{s^2+\alpha s+1}\right)V_i$$

transfer function notch filter

$$\frac{V_N}{V_i} = \frac{s^2+1}{s^2+\alpha s+1}$$

Second order LPF



Y = admittance $= \frac{1}{R}$

Sallen key filter

Since op-amp is connected in non-inverting mode

$$V_o = \left(1 + \frac{R_f}{R_i}\right) V_B$$

where $A_o = 1 + \frac{R_f}{R_i}$

$$V_o = A_o V_B \quad \hookrightarrow (1)$$

Apply KCL at node A.

$$(V_A - V_i)Y_1 + (V_A - V_B)Y_2 + (V_A - V_o)Y_3 = 0$$

$$V_A Y_1 - V_i Y_1 + V_A Y_2 - V_B Y_2 + V_A Y_3 - V_o Y_3 = 0$$

$$V_A (Y_1 + Y_2 + Y_3) - V_i Y_1 - V_B Y_2 - V_o Y_3 = 0$$

$$V_A (Y_1 + Y_2 + Y_3) - V_B Y_2 - V_o Y_3 = V_i Y_1 \quad \hookrightarrow (2)$$

Substitute (1) in (2)

$$V_A (Y_1 + Y_2 + Y_3) - \frac{V_o}{A_o} Y_2 - V_o Y_3 = V_i Y_1 \quad \hookrightarrow (3)$$

At node B, KCL

$$(V_B - V_A)Y_2 + V_B Y_4 = 0$$

$$V_B Y_2 - V_A Y_2 + V_B Y_4 = 0$$

$$V_B (Y_2 + Y_4) - V_A Y_2 = 0$$

$$V_A = \frac{V_B}{Y_2} (Y_2 + Y_4)$$

$$\frac{\quad}{Y_2}\,(12\cdot 4)$$

$$V_A = \frac{V_0}{A_0}\left(\frac{Y_2+Y_4}{Y_2}\right) \rightarrow (4)$$

Substitute (4) in (3)

$$V_i Y_1 = \frac{V_0}{A_0}\left(\frac{Y_2+Y_4}{Y_2}\right)(Y_1+Y_2+Y_3) - \frac{V_0}{A_0}Y_2 - V_0 Y_3$$

$$= \frac{V_0(Y_2+Y_4)(Y_1+Y_2+Y_3) - V_0 Y_2^2 - V_0 A_0 Y_3 Y_2}{A_0 Y_2}$$

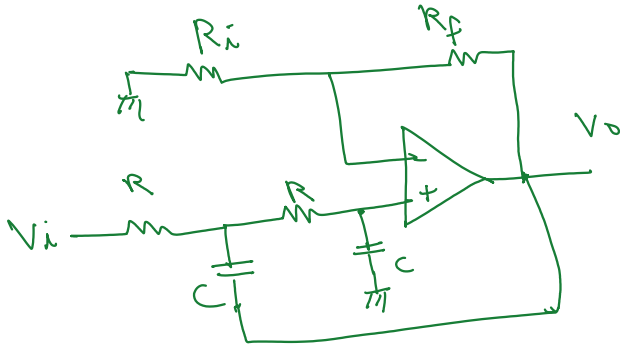
$$= \frac{V_0}{A_0 Y_2}\left[Y_1Y_2 + Y_2^2 + Y_2Y_3 + Y_1Y_4 + Y_2Y_4 + Y_3Y_4 - Y_2^2 - A_0 Y_2 Y_3\right]$$

$$V_i Y_1 = \frac{V_0}{A_0 Y_2}\left[Y_1Y_2 + Y_2Y_3(1-A_0) + Y_4(Y_1+Y_2+Y_3)\right]$$

$$\frac{V_0}{V_i} = \frac{A_0 Y_2 Y_1}{Y_1Y_2 + Y_2Y_3(1-A_0) + Y_4(Y_1+Y_2+Y_3)}$$

General expression

Second order lowpass circuit



$$Y_1 = Y_2 = \frac{1}{R}$$

$$Y_3 = Y_4 = \frac{1}{sC}$$

$$V_0 = A_0\left(\frac{1}{R}\right)\left(\frac{1}{R}\right)$$

$$H(s) = \frac{V_o}{V_i} = \frac{A_o\left(\frac{1}{R}\right)\left(\frac{1}{R}\right)}{\left(\frac{1}{R}\right)\left(\frac{1}{R}\right) + \left(\frac{1}{R}\right)(sC)(1-A_o) + sC\left(\frac{1}{R}+\frac{1}{R}+sC\right)}$$

$$= \frac{\frac{A_o}{R^2}}{\frac{1}{R^2} + \frac{sC}{R}(1-A_o) + sC\left(\frac{2}{R}+sC\right)}$$

$$= \frac{A_o/R^2}{\frac{1}{R^2} + \frac{sC}{R}(1-A_o) + sC\left(\frac{2+sCR}{R}\right)}$$

$$= \frac{\frac{A_o}{R^2}}{\frac{1+sRC(1-A_o)+2sRC+s^2R^2C^2}{R^2}}$$

$$= \frac{A_o}{1+sRC(1-A_o)+sRC(2+sRC)}$$

$$= \frac{A_o}{1+sRC(3-A_o+sRC)}$$

$$H(s) = \frac{A_o}{1+sRC(3-A_o)+(sRC)^2}$$

When $s=0$ $\quad H(s) = A_o$

$s=\infty$ $\quad H(\infty) = 0$

Let $\omega_1 = \frac{1}{RC}$ and $\alpha = 3-A_o$

$$H(s) = \frac{A_o}{1+\frac{s}{(\alpha)}+\left(\frac{s}{\omega_1}\right)^2}$$

$$H(s) = \frac{A_0}{1 + \frac{s}{\omega_h}(\alpha) + \left(\frac{s}{\omega_h}\right)^2}$$

$$H(s) = \frac{A_0\,\omega_h^2}{s^2 + s\omega_h\alpha + \omega_h^2}$$

$s = j\omega$

$$H(j\omega) = \frac{A_0\,\omega_h^2}{(j\omega)^2 + (j\omega)\omega_h\alpha + \omega_h^2}$$

$$= \frac{A_0}{\frac{(j\omega)^2}{\omega_h^2} + j\omega\frac{\omega_h\alpha}{\omega_h^2} + \frac{\omega_h^2}{\omega_h^2}}$$

$$= \frac{A_0}{\frac{-\omega^2}{\omega_h^2} + j\frac{\omega\alpha}{\omega_h} + 1}$$

$$= \frac{A_0}{1 - \frac{\omega^2}{\omega_h^2} + j\frac{\omega\alpha}{\omega_h^2}}$$

$$|H(j\omega)| = \frac{A_0}{\sqrt{\left(1 - \frac{\omega^2}{\omega_h^2}\right)^2 + \left(\frac{\omega\alpha}{\omega_h}\right)^2}} \quad \rightarrow (A)$$

put $s_n = \frac{j\omega}{\omega_h}$

$$H(s_n) = \frac{A_0}{s_n^2 + s_n\alpha + 1}$$

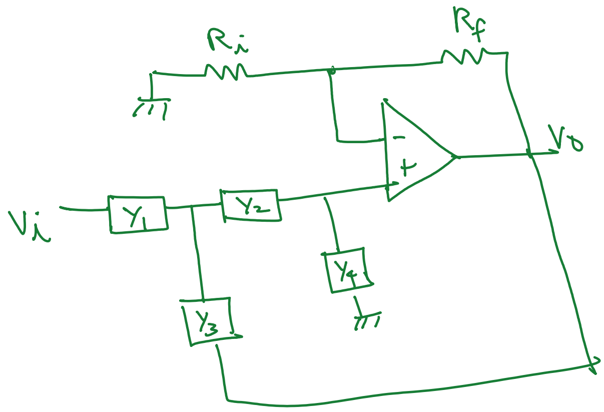
Butterworth filter, $\alpha = 1.414$

put $\alpha = 1.414$ in eqn (A)

$$|H(j\omega)| = \frac{A_0}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^4}}$$

$$\sqrt{1+\left(\frac{\omega}{\omega_h}\right)^4}$$

Second order HPF



$$Y_1 = sC_1 \quad Y_2 = sC_2 \quad Y_3 = \frac{1}{R_1} \quad Y_4 = \frac{1}{R_2}$$

General expression

$$\frac{V_o}{V_i} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_o)}$$

$$= \frac{A_o (sC_1)(sC_2)}{(sC_1)(sC_2) + \frac{1}{R_2}\left(sC_1 + sC_2 + \frac{1}{R_1}\right) + sC_2\left(\frac{1}{R_1}\right)(1 - A_o)}$$

$$= \frac{A_o s^2 C_1 C_2}{s^2 C_1 C_2 + \frac{1}{R_2}\left(sC_1 + sC_2 + \frac{1}{R_1}\right) + \frac{sC_2}{R_1}(1 - A_o)}$$

Divide numerator and denominator by $C_1 C_2$

$$= \frac{A_o s^2}{s^2 + \frac{1}{R_2 C_1 C_2}\left(sC_1 + sC_2 + \frac{1}{R_1}\right) + \frac{s}{R_1 C_1}(1 - A_o)}$$

$$= \frac{A_o s^2}{s^2 + \frac{sC_1 + sC_2}{R_2 C_1 C_2} + \frac{1}{R_1 R_2 C_1 C_2} + \frac{s}{R_1 C_1}(1 - A_o)}$$

$$= \frac{A_o s^2}{\quad}$$

$$= \frac{A_0 s^2}{s^2 + s\left(\frac{R_1C_1 + sR_1C_2 + 1 + sR_2C_2(1-A_0)}{R_1R_2C_1C_2}\right)}$$

$$= \frac{A_0 s^2}{s^2 + s\left(\frac{R_1C_1 + R_2C_2 + R_2C_2(1-A_0)}{R_1R_2C_1C_2}\right) + \frac{1}{R_1R_2C_1C_2}}$$

→ (A)

$$V_0 = \left(1 + \frac{R_f}{R_i}\right) V_B$$

$$\frac{V_0}{V_B} = A_0 = 1 + \frac{R_f}{R_i}$$

General transfer function

$$\frac{V_0}{V_i} = \frac{A_0 s^2}{s^2 + \alpha\omega_0 s + \omega_0^2} \quad \rightarrow (B)$$

Compare (A) and (B)

$$\omega_0^2 = \frac{1}{R_1R_2C_1C_2}$$

$$\omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}}$$

$$\alpha\omega_0 = \frac{R_1C_1 + R_1C_2 + R_2C_2(1-A_0)}{R_1R_2C_1C_2}$$

$$\alpha \frac{1}{\sqrt{R_1R_2C_1C_2}} = \frac{R_1C_1 + R_2C_2 + R_2C_2(1-A_0)}{R_1R_2C_1C_2}$$

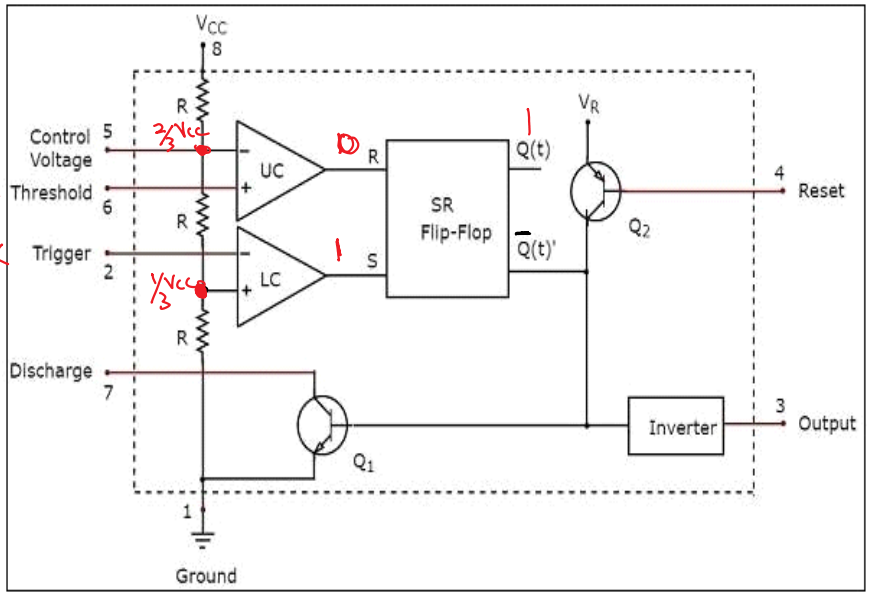
Let $R_1 = R_2 = R$ & $C_1 = C_2 = C$

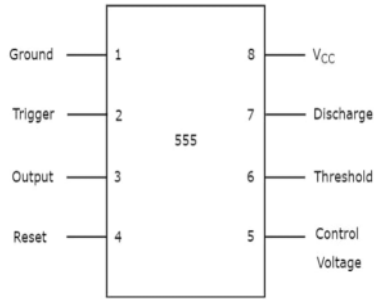
$$\omega \frac{1}{\sqrt{R^2C^2}} = \frac{RC + RC + RC(1-A_0)}{R^2C^2}$$

$$\frac{\omega}{RC} = \frac{RC(1+1+1-A_0)}{R^2C^2}$$

$$\boxed{\omega = 3 - A_0}$$

Timer IC 555: Functional diagram





$V_{cc}\,\frac{2R}{R+2R} = \frac{2}{3}V_{cc}$

$V_{cc}\,\frac{R}{2R+R} = \frac{1}{3}V_{cc}$

- The voltage divider network consists of a three 5KΩ resistors that are connected in series between the supply voltage Vcc and ground. It provides 2/3 Vcc to the upper comparator and 1/3 Vcc to the lower comparator

By changing the voltage at these pins, we can change the output of the comparator

Whenever threshold voltage goes above this $\frac{2}{3}V_{cc}$ the output of comparator will become high

Whenever the trigger voltage goes below $\frac{1}{3}V_{cc}$ the output of comparator will become high.

When we want to change the state of the Comparator, then we need to change the trigger signal in such a way that Pin 2 voltage goes below the $\frac{1}{3}V_{cc}$ voltage

S	R	Q_n	Q_{n+1}
0	0	0/1	0/1
0	1	0/1	0
1	0	0/1	1
1	1	0/1	X

⇒ Let trigger signal at Vcc.

The o/p of Second Comparator is at logic 0

ie, S = 0

Assume initially the threshold voltage is less than the reference voltage $\frac{2}{3}V_{cc}$.

∴ o/p of first comparator is zero

ie, R=0

Thus the o/p of FF will remain as it is.

⇒ When threshold voltage goes above this $\frac{2}{3}V_{cc}$ voltage, the output of comparator 1 will logic 1. Then o/p of FF is logic 0. The o/p of 555 timer is also zero.

By threshold voltage we are controlling the o/p.

⇒ Assume the threshold voltage is less than reference voltage $\frac{2}{3}V_{cc}$

∴ o/p of comparator 1 is zero

Whenever the trigger signal goes below the $\frac{1}{3}V_{cc}$, the o/p of comparator 2 will be high

ie, R=0 S=1

∴ FF will set to logic 1

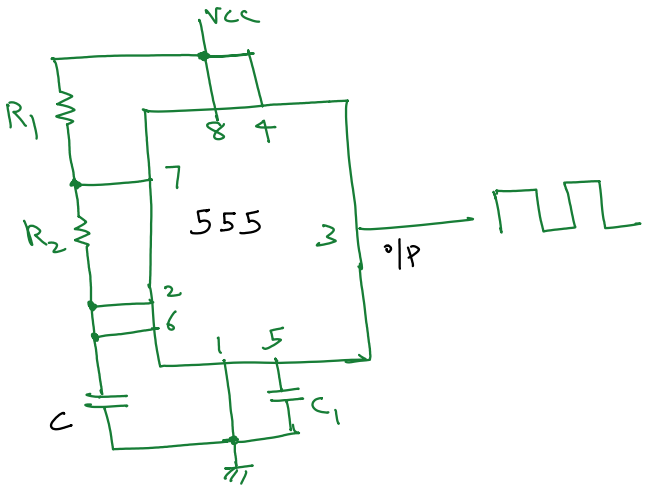
o/p will also set to logic 1

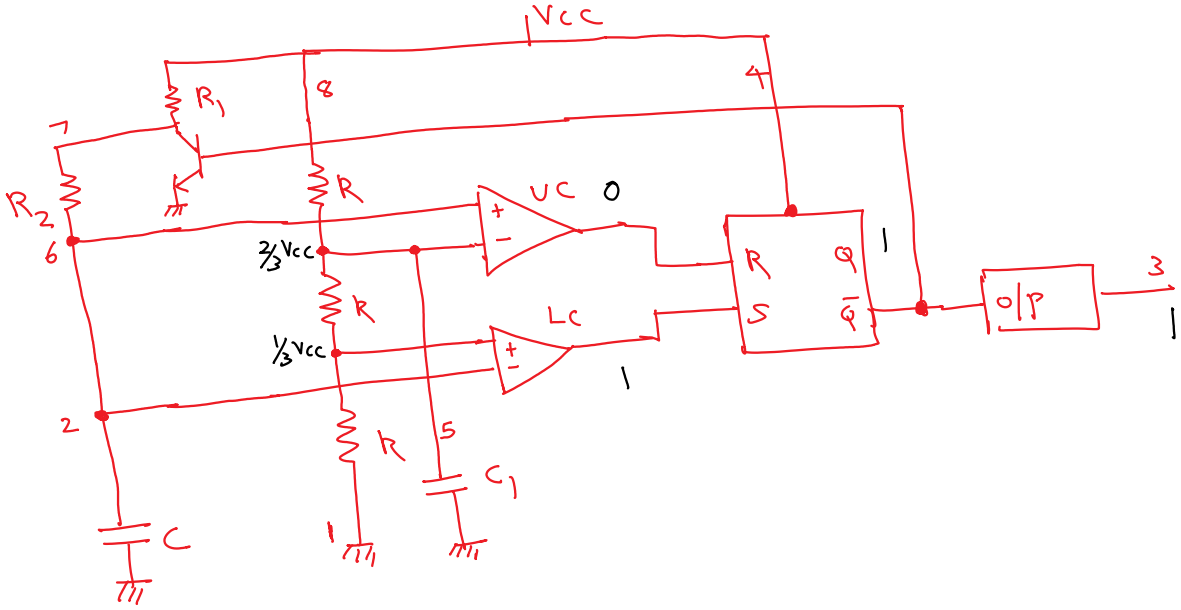
⇒ Thus using threshold and trigger pin we are controlling the o/p voltage and hence the timing of o/p signal.

⇒ using pin 5, we can also control timing.

⇒ To change the input voltage to the threshold pin, the external resistor and capacitors are connected between the threshold and discharge pin through the supply voltage. Similarly for trigger pin.

Astable Multivibrator using 555 timer





⇒ When circuit is turned on, the capacitor is fully uncharged so that voltage at Pin 2 and 6 is zero.

⇒ Initially the Lower comparator at logic 1 and Upper comparator at logic 0. Because the voltage at inverting terminal (pin 2) is low than 1/3 Vcc for lower comparator and the voltage at non inverting terminal (pin 6) is low than 2/3 Vcc.

So S = 1 R = 0

∴ o/p of FF = 1

∴ o/p of 555 timer = 1

Since Q = 1 $\bar{Q}$ = 0 so the transistor is in OFF

Condition. The capacitor C starts charging through R_1 and R_2.

The voltage at pin 2 and 6 will start increasing

⇒ whenever the voltages at pin 2 crosses $\frac{1}{3}V_{cc}$, the o/p of lower comparator will become logic 0 because the voltage at inverting node will be slightly more than voltage at non-inverting terminal.

while the voltage at pin 6 is still less than $\frac{2}{3}V_{cc}$ the o/p of upper comparator is at logic 0.

ie, S = 0 R = 0

o/p of FF will retain previous state.

∴ Q goes to logic 1

o/p of 555 timer = logic 1

⇒ when the capacitor voltage crosses $\frac{2}{3}V_{cc}$, o/p of upper comparator goes high.

Now S = 0 R = 1

o/p of FF reset to logic 0.

ie, whenever the capacitor voltage reaches $\frac{2}{3}V_{cc}$, the transition in o/p from logic high to logic low value.

⇒ when Q = 0 $\bar{Q}$ = 1, transistor ON.

The capacitor C starts discharging through the transistor. The voltage across capacitor starts reducing.

As the voltage (pin 6) goes below $\frac{2}{3}V_{cc}$, the o/p of upper comparator become logic 0.

The o/p of second comparator will also be 0.

ie, S=0 R=0

FF will retain its previous state ie, Q=0

o/p of 555 timer will also be zero

⇒ During discharging, whenever the voltage across capacitor goes below $\frac{1}{3}V_{cc}$, o/p of low comparator is at logic 1

ie, S=1 R=0

FF will set to 1

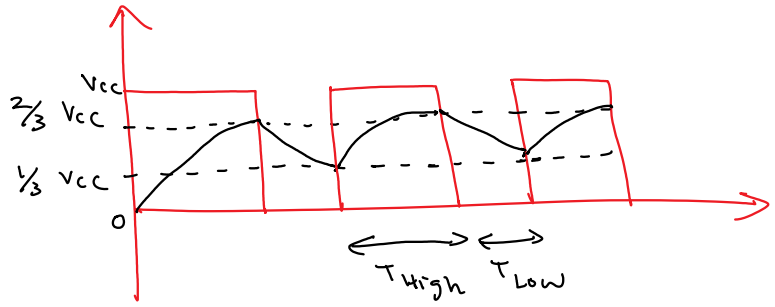
o/p transition to logic high

As Q=1 $\bar{Q}$=0, transistor OFF, capacitor again starts charging through R_1 and R_2

⇒ Thus capacitor is charging between $\frac{2}{3}V_{cc}$ and $\frac{1}{3}V_{cc}$. and because of charging and discharging of capacitor, we can see a transition in the o/p.

⇒ During charging process the voltage across capacitor just crosses $\frac{2}{3}V_{cc}$ voltage, the transition of o/p from logic high to logic zero value

⇒ During discharging process, the voltage across capacitor goes below $\frac{1}{3}V_{cc}$, the transition of o/p from logic low to logic high value.



T_{High} → time required for capacitor to charge from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$

The capacitor voltage for a lowpass RC circuit to i/p V_{cc} is

$$v_c = V_{cc}\left(1-e^{-t/RC}\right) \quad \checkmark$$

$1-e^{-t_1/RC} = \frac{2}{3}$

t_1 is the time taken for capacitor to charge from 0 to $\frac{2}{3}V_{cc}$.

$$\frac{2}{3}V_{cc} = V_{cc}\left(1-e^{-t_1/RC}\right) \Rightarrow t_1 = 1.09RC \hookrightarrow (1)$$

t_2 is the time to charge from 0 to $\frac{1}{3}V_{cc}$

$$\frac{1}{3}V_{cc} = V_{cc}\left(1-e^{-t_2/RC}\right)$$

$$\Rightarrow t_2 = 0.405RC \hookrightarrow (2)$$

$$T_{High} = t_1 - t_2$$

$$= 1.09RC - 0.405RC$$

$$= \underline{0.69RC}$$

$$T_{High} = 0.69(R_A + R_B)C$$

o/p is low while capacitor discharges from $\frac{2}{3}V_{cc}$ to $\frac{1}{3}V_{cc}$ and Voltage across capacitor is

$$\frac{1}{3}V_{cc} = \frac{2}{3}V_{cc}\,e^{-t/RC}$$

$$\Rightarrow t = 0.69RC$$

$$T_{low} = 0.69R_2C$$

$$T = T_{High} + T_{Low}$$

$$= 0.69 (R_1 + R_2) C + 0.69 R_2 C$$

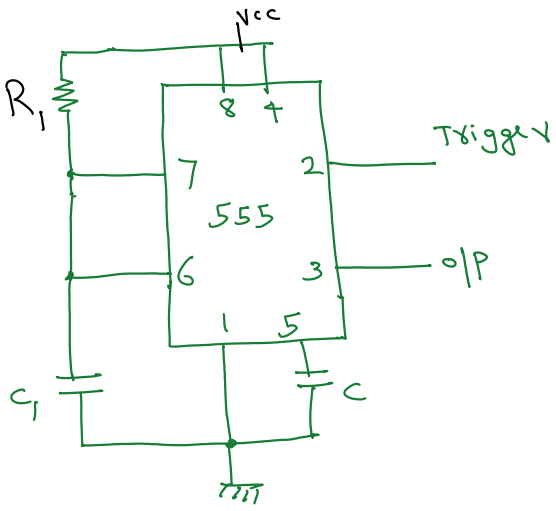
$$= 0.69 (R_1 + 2R_2) C$$

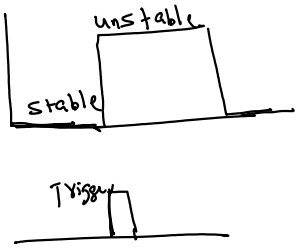
$$f = \frac{1}{T} = \frac{1.45}{(R_1 + 2R_2) C}$$

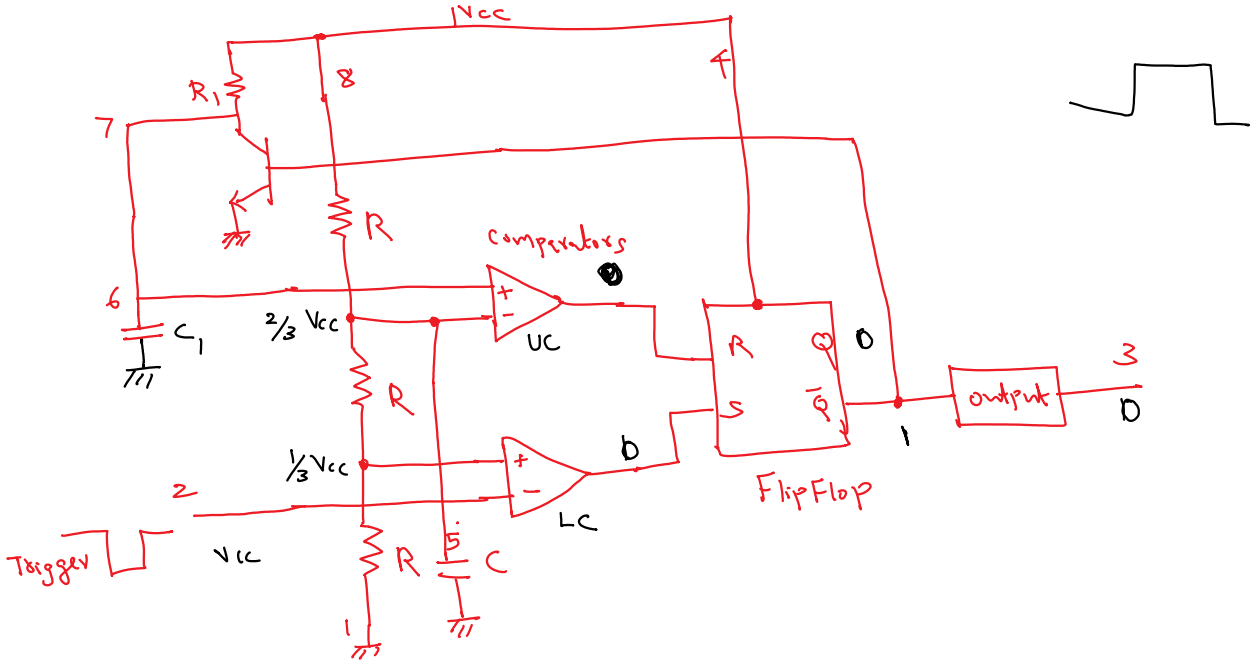
$$\text{Duty cycle } \% = \frac{T_{low}}{T} \times 100 = \frac{T_{low}}{T_{low} + T_{high}} \times 100$$

$$= \frac{R_2}{R_1 + 2R_2} \times 100$$

Monostable Multivibrator







⇒ Let us assume the output of 555 timer is zero.

When o/p is zero, $\bar{Q} = 1$ and transistor is ON.

The pin 6 and 7 is at ground potential

The upper comperator output will be at zero since the voltage at inverting terminal ($\frac{2}{3}$ Vcc) is greater than non inverting terminal (0).

The lower comparator output will also be at zero since the voltage at inverting terminal (will be at Vcc if no trigger is applied) is greater than non inverting terminal ($\frac{1}{3}$ Vcc).

ie, R = 0 S = 0

∴ The o/p of FF will remain in previous condition

In this condition, o/p of 555 timer is zero

⇒ whenever we apply trigger signal in such a way that o/p of pin 2 goes below the reference voltage.

The o/p of Lower comparator will become logic 1.

Since $\bar{Q} = 1$, pin 6 will remain at ground potential.

So, o/p of upper comparator will remain at logic 0.

ie, $S = 1 \quad R = 0$ (during trigger)

∴ o/p of FF = logic 1

∴ o/p of timer = logic 1

ie, $Q = 1 \quad \bar{Q} = 0$

Thus transistor turns OFF.

Capacitor C_1 starts charging towards V_{cc}.

⇒ After triggering action completes, the voltage at pin 2 becomes V_{cc}.

o/p of Lower comparator becomes logic zero.

During charging of C_1, whenever the voltage at pin 6 just crosses $\frac{2}{3} V_{cc}$, the o/p of upper comparator will become logic 1.

ie, $S = 0 \quad R = 1$

The o/p of FF = logic 0

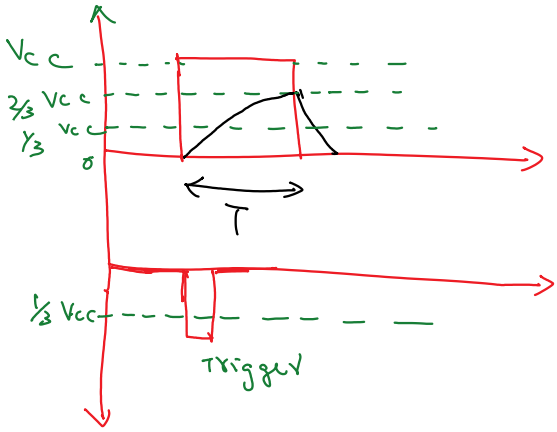
o/p of 555 timer = logic 0

In this way o/p of 555 timer goes into unstable state.

⇒ whenever the capacitor voltage just reaches the $\frac{2}{3} V_{cc}$ voltage then the o/p will come to stable state.

As soon as Q will become zero, $\bar{Q}$ will become 1, the transistor turn on, the capacitor gets discharged through transistor path.

Thus the o/p of comparators will become logic 0.



Whenever the triggering action happens, ie, whenever the voltage at pin 2 just go below $\frac{1}{3}V_{cc}$ voltage, the o/p of 555 timer will go to the logic high value.
At that time capacitor starts charging towards V_{cc}.

As soon as the voltage across capacitor crosses $\frac{2}{3}V_{cc}$ then the o/p of 555 timer will become logic 0.
Capacitor gets discharged through transistor.

The voltage across capacitor

$$V_c = V_{cc}\left(1-e^{-t/RC}\right)$$

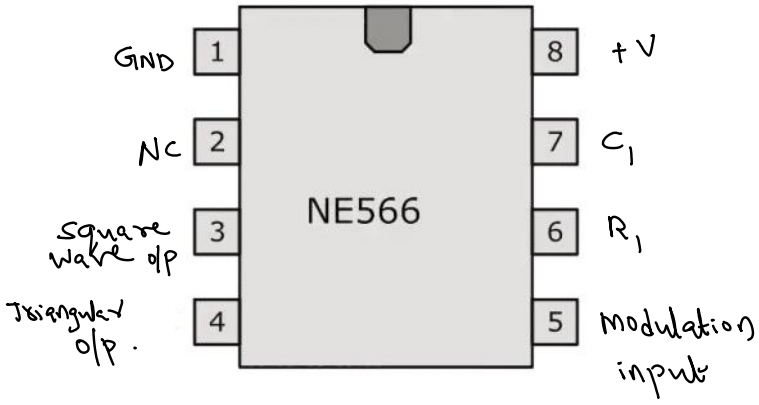
at $t = T$ $V_c = \frac{2}{3}V_{cc}$

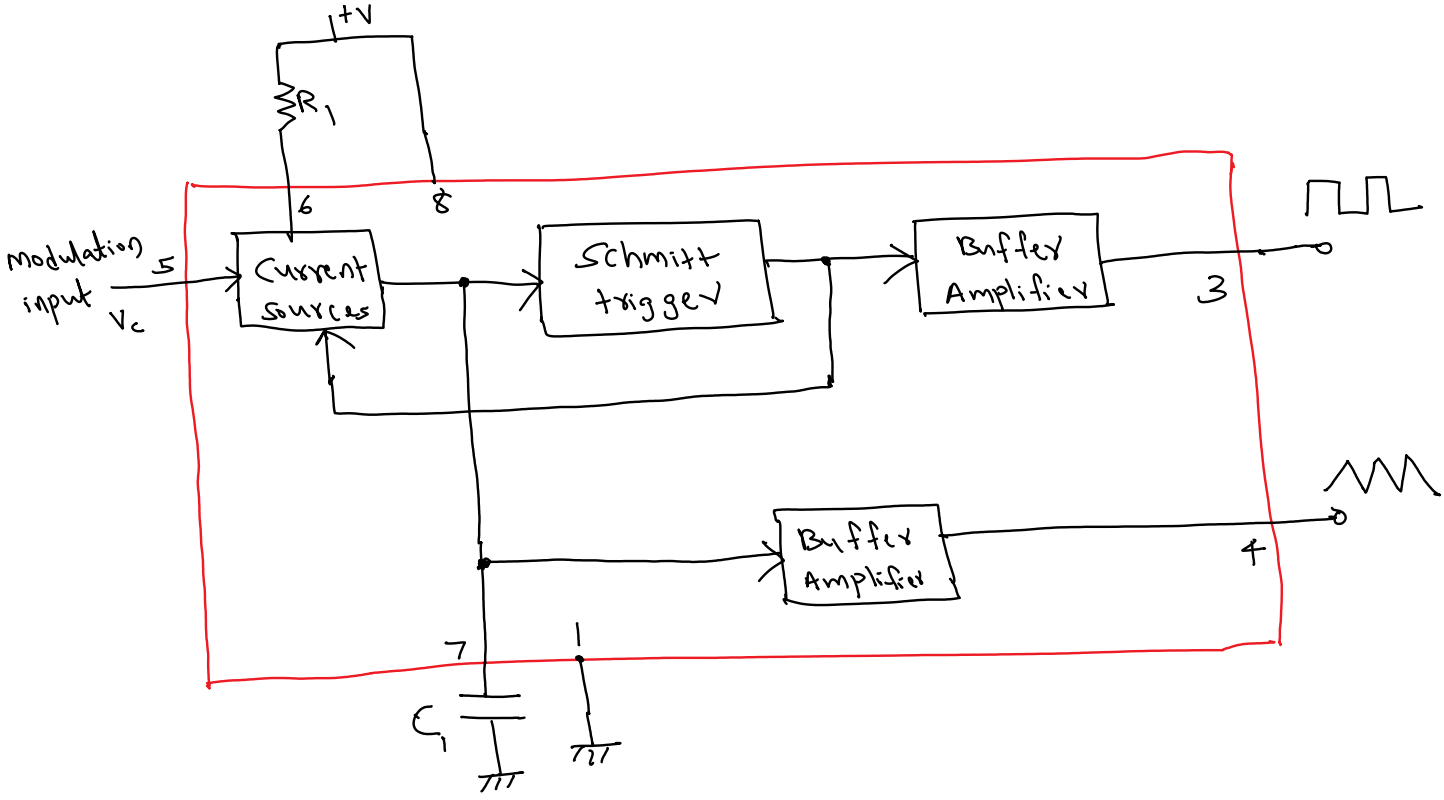
$$\therefore \frac{2}{3}V_{cc} = V_{cc}\left(1-e^{-T/R_1C_1}\right)$$

$$T = R_1C_1 \ln\left(\tfrac{1}{3}\right)$$

$$T = 1.1\,R_1C_1$$

Voltage Controlled oscillator





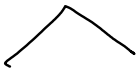
A voltage-controlled oscillator (VCO) is an electronic oscillator whose frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency.

Applications:
FM modulators
FSK modulators
Signal generators

The frequency of oscillation is determined by an external resistor R1 and capacitor C1, and the voltage Vc applied to the control terminal 5.

The triangular wave is generated by alternately charging the external capacitor C1 by one current source and linearly discharging it by another. The charge and discharge levels are determined by the Schmitt trigger action. The Schmitt trigger also provides square wave output.

Both the outputs are buffered so that output impedance of each is 50 ohm



Phase-Locked Loops (PLL)

A phase-locked loop or phase lock loop is a control system that generates an output signal whose phase is related to the phase of an input signal.

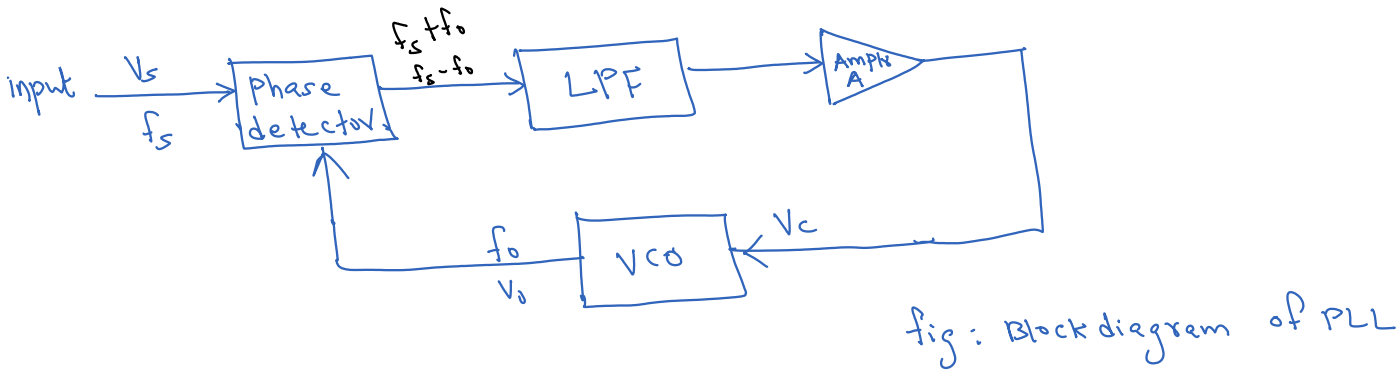


fig : Block diagram of PLL

The VCO is a free running oscillator and operates at a set frequency called free running frequency. This frequency is determined by the external timing capacitor and an external resistor.
The frequency deviation is directly proportional to the dc control voltage and hence it is called voltage controlled oscillator.

If an input signal Vs of frequency fs is applied to the PLL, the phase detector compares the phase and frequency of the input signal to that of the output Vo of the VCO.
If the two signals differ in frequency and/or phase, an error voltage Ve is generated.

The phase detector is basically a multiplier and produces the sum (fs+fo) and (fs-fo) components at its output.
The high frequency component fs+fo is removed by the LPF and the difference frequency component is amplified and then applied as control voltage to VCO.

The signal Vc shifts the VCO frequency in a direction to reduce the frequency difference between fs and fo.
Once this action starts, the signal is in the capture range.

The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency .
The circuit is said to be locked.

Once locked, the output frequency fo of VCO is identical to fs except for a finite phase difference Φ. This phase difference generates a corrective control voltage Vc to shift the VCO frequency from fo to fs thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal.

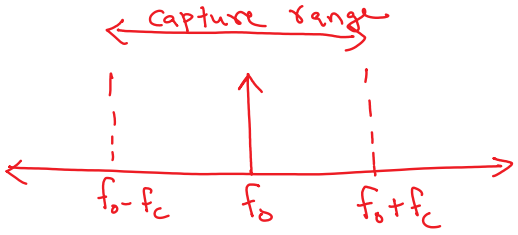
PLL goes through three stages
1. Free running
2. Capture
3. Locked or tracking

Lock in range: Once the PLL is locked, it can track frequency changes in the incoming signals.
The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range. The lock range is usually expressed as a percentage of fo, the VCO frequency.

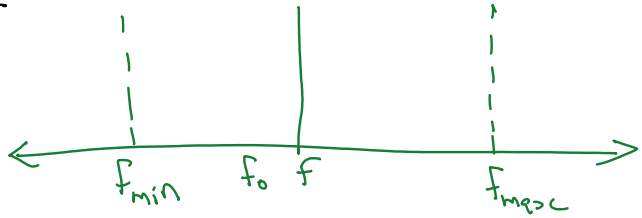
Capture range: The range of frequencies over which the PLL can acquire lock with an input signal is called capture range.
The capture range is also expressed as a percentage of fo, the VCO frequency.

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time.

Capture range



Lock range



Let VCO is locked to i/p frequency f

If i/p frequency f changes, then the VCO will follow that frequency provided the input frequency is within the lock range.

If i/p frequency f goes out of lock range, then the VCO starts running at free running frequency f_0.

Phase detector

Let α and β are the phases of two signals

phase difference $= \alpha - \beta$

if $\alpha - \beta$ is very small

$\approx \sin(\alpha - \beta)$

$\simeq \sin\alpha\cos\beta - \sin\beta\cos\alpha$

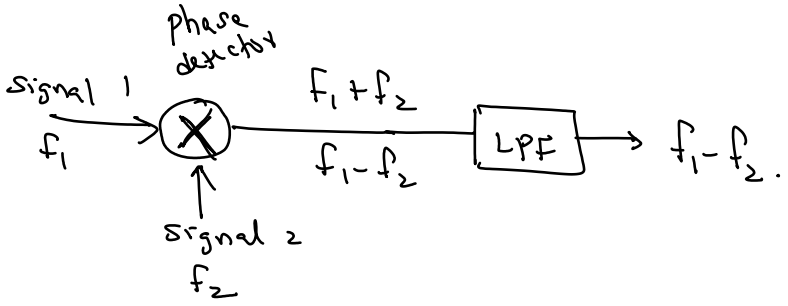
we have $\sin\alpha\cos\beta = \sin\frac{(\alpha-\beta)}{2} + \sin\frac{(\alpha+\beta)}{2}$

$\Downarrow$

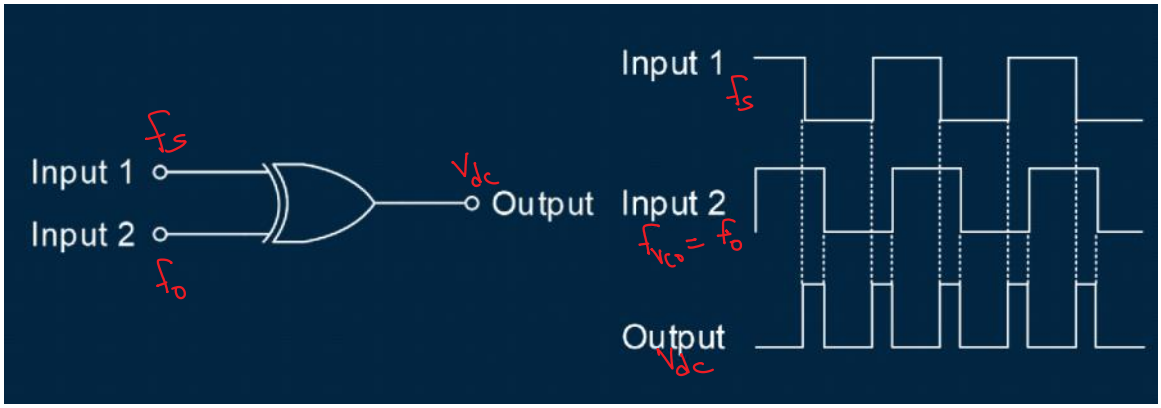
high freq component

$\Downarrow$

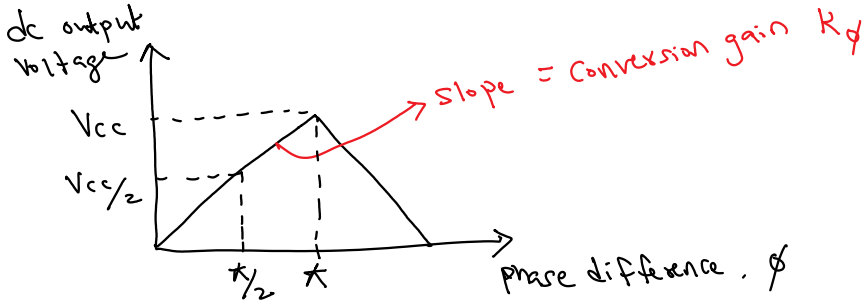
eliminated by LPF



Phase Detector



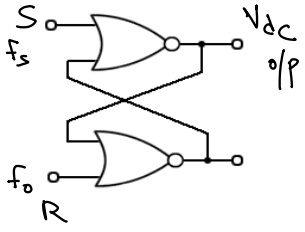
The output of the XOR gate is high when one of the input signals fs or fo is high. This type of detector is used when both the input signals are square waves. The output wave form for fs=fo is shown in fig. In this figure, fs is leading fo by Φ degrees.

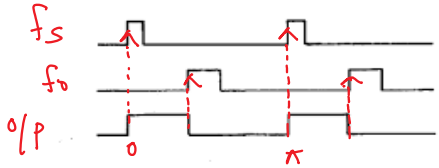


The maximum dc output voltage occurs when phase difference is π.
The slope of the curve,

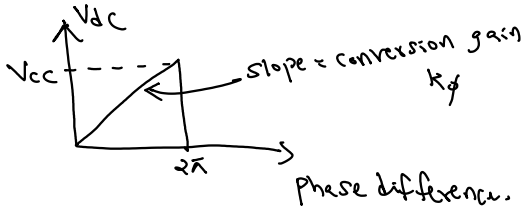
$$K_\phi = \frac{V_{cc}}{\pi} = \frac{5}{\pi} = 1.59 \text{ V/rad}$$

Another type of phase detector is an edge triggered phase detector.





Edge triggered phase detector
using CD4001, 2 input NOR gate.



This circuit is useful when fs and fo are both pulse waveforms with duty cycle less than 50percent.
This has better capture range and locking characteristics as the output characteristics is linear upto 360

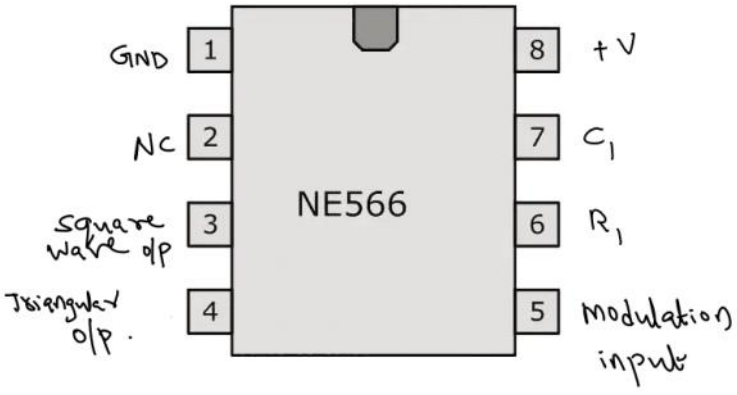
degree.

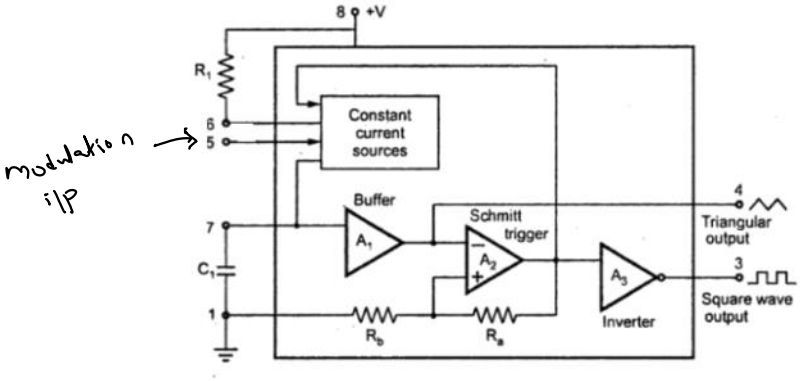
VCO: LM 566

A Voltage-Controlled Oscillator (VCO) is a circuit that provides a varying output signal (typically of square-wave or triangular-wave form) whose frequency can be adjusted over a range controlled by an externally applied DC voltage.

The VCO provides a linear relationship between the applied voltage and the oscillation frequency. The applied voltage is called control voltage. The control of frequency with the help of control voltage is known as voltage to frequency conversion. Hence VCO is otherwise known as Voltage to frequency converter.

Practically VCO is available in IC form. IC 566 (LM566/SE566) from Signetics is a popular VCO. IC 566 contains circuitry to generate both square wave and triangular-wave signals whose frequency is set by an external resistor and capacitor and then varied by an applied dc voltage.





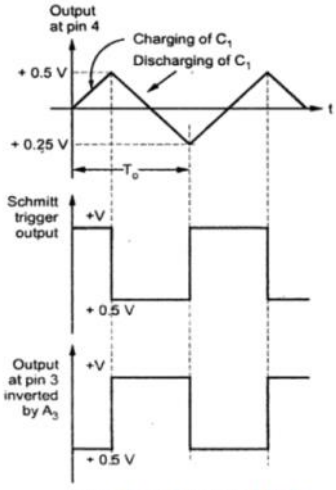


Fig. Wave forms of VCO

A Schmitt trigger circuit is used to switch the current sources between charging and discharging the capacitor, and the triangular voltage developed across the capacitor and square wave from the Schmitt trigger are provided as outputs through buffer amplifiers.

The Voltage Vc is applied to the modulation input pin which is a control voltage.

The capacitor C1 is linearly charged or discharged by a constant current source.

The charging current can be controlled by controlling the voltage Vc at pin 5 or by varying the resistance R1 which is external to the IC.

The charging and discharging levels are determined by the Schmitt trigger

The output voltage of Schmitt trigger is designed to swing between +V and 0.5V

For Ra= Rb, the voltage at non-inverting terminal swings between 0.5(+V) to 0.25(+V).

Thus the triangular wave is generated due to alternate charging and discharging of the capacitor C1 in linear manner.

When C1 voltage increases beyond 0.5(+V), the ST output goes low, and the capacitor starts discharging.

When the voltage becomes less than 0.25(+V), the output of the ST goes high.

Due to similar current sources used for charging and discharging, the time taken by C1 to charge and discharge is same. This produces exact triangular wave.

The output of the ST is step response, which is a square wave output.

Free running frequency.

$$f_o = \frac{2}{R_1 \times C_1} \times \left(\frac{V^+ - V_C}{V^+}\right)$$

Lowpass Filter

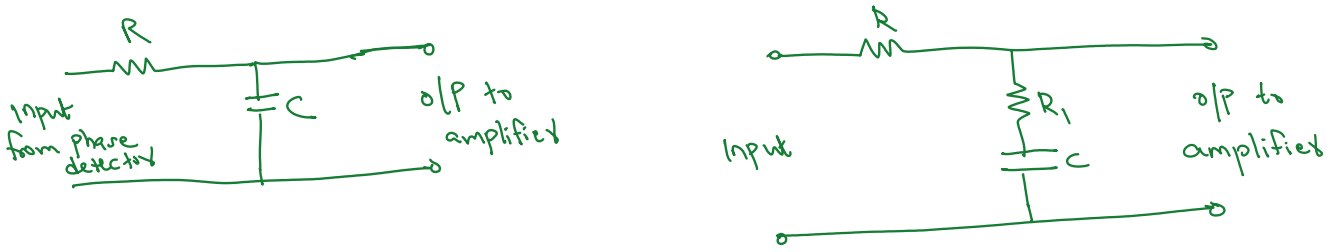


fig: passive filter.

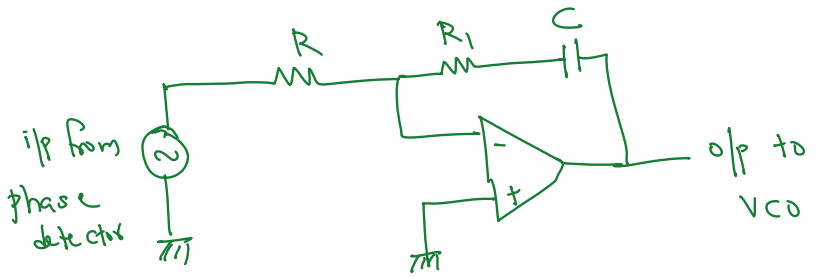


fig: Active filter.

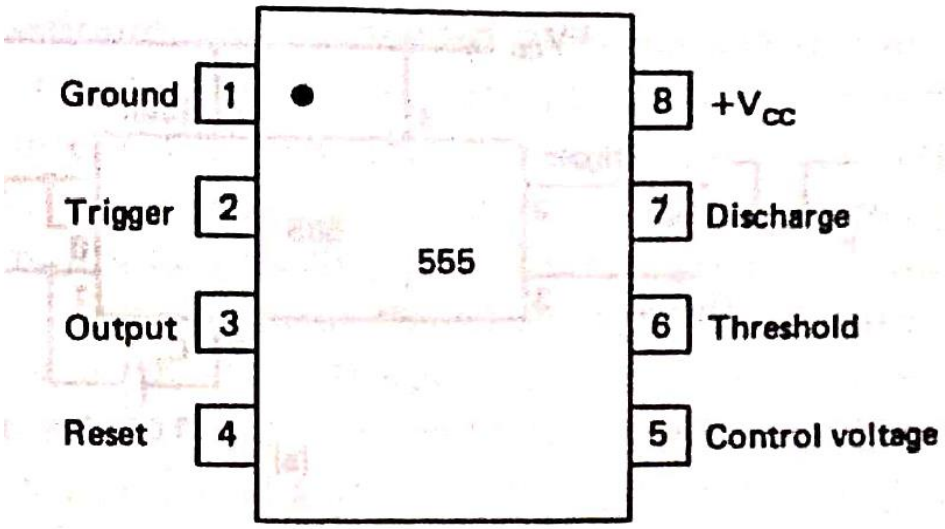
Removes the high frequency components and noise.

It controls dynamic characteristics like capture range, lock range ,bandwidth and transient response of the PLL.

If filter bandwidth is reduced, response time increases.
Reducing the filter bandwidth reduces the capture range.

The charge on the filter capacitor gives a short time memory to the PLL.

555 Timer



- Pin 1. – **Ground**, The ground pin connects the 555 timer to the negative (0v) supply rail.

- Pin 2. – **Trigger**, The negative input to comparator No 1. A negative pulse on this pin "sets" the internal Flip-flop when the voltage drops below 1/3Vcc causing the output to switch from a "LOW" to a "HIGH" state.

- Pin 3. – **Output**, The output pin can drive any TTL circuit and is capable of sourcing or sinking up to 200mA of current at an output voltage equal to approximately Vcc – 1.5V so small speakers, LEDs or motors can be connected directly to the output.

- Pin 4. – **Reset**, This pin is used to "reset" the internal Flip-flop controlling the state of the output, pin 3. This is an active-low input and is generally connected to a logic "1" level when not used to prevent any unwanted resetting of the output.

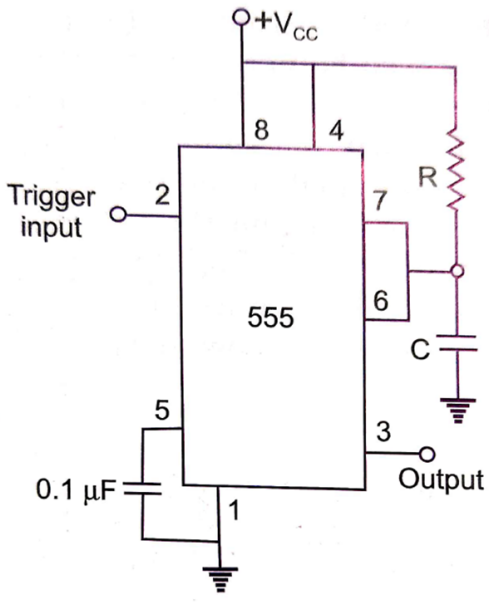
- Pin 5. – **Control Voltage**, This pin controls the timing of the 555 by overriding the 2/3Vcc level of the voltage divider network. By applying a voltage to this pin the width of the output signal can be varied independently of the RC timing network. When not used it is connected to ground via a 10nF capacitor to eliminate any noise.

- Pin 6. – **Threshold**, The positive input to comparator No 2. This pin is used to reset the Flip-flop when the voltage applied to it exceeds 2/3Vcc causing the output to switch from "HIGH" to "LOW" state. This pin connects directly to the RC timing circuit.

- Pin 7. – **Discharge**, The discharge pin is connected directly to the Collector of an internal NPN transistor which is used to "discharge" the timing capacitor to ground when the output at pin 3 switches "LOW".

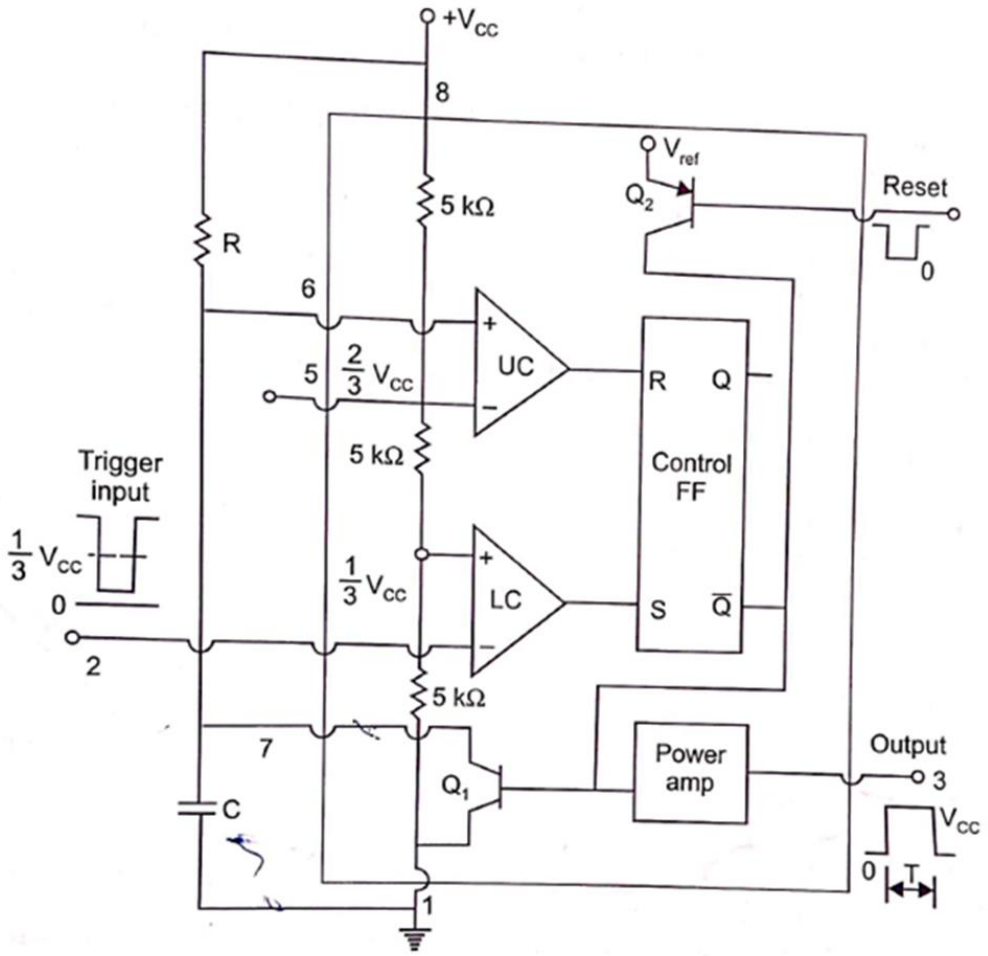
- Pin 8. – **Supply +Vcc**, This is the power supply pin and for general purpose TTL 555 timers is between 4.5V and 15V.

Monostable Multivibrator using 555



Monostable multivibrator

Monostable Multivibrator using 555



The **Monostable 555 Timer** circuit triggers on a negative-going pulse applied to pin 2 and this trigger pulse must be much shorter than the output pulse width allowing time for the timing capacitor to charge and then discharge fully. Once triggered, the 555 Monostable will remain in this "HIGH" unstable output state until the time period set up by the $R_1 \times C_1$ network has elapsed. The amount of time that the output voltage remains "HIGH" or at a logic "1" level, is given by the following time constant equation.

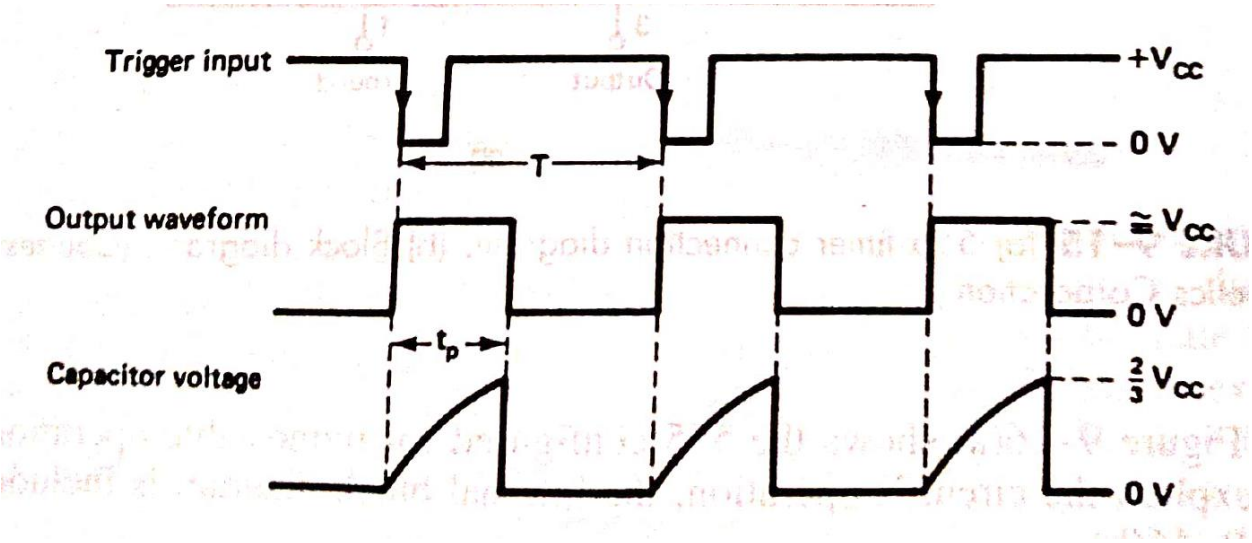
$$\tau = 1.1 R_1 C_1$$

A **Monostable 555 Timer** is required to produce a time delay within a circuit. If a 10uF timing capacitor is used, calculate the value of the resistor required to produce a minimum output time delay of 500ms.

500ms is the same as saying 0.5s so by rearranging the formula above, we get the calculated value for the resistor, R as:

$$R = \frac{t}{1.1C} = \frac{0.5}{1.1 \times 10uF} = \frac{0.5}{1.1 \times 10 \times 10^{-6}} = 45.5k\Omega$$

The calculated value for the timing resistor required to produce the required time constant of 500ms is therefore, 45.5KΩ. However, the resistor value of 45.5KΩ does not exist as a standard value resistor, so we would need to select the nearest preferred value resistor of 47kΩ

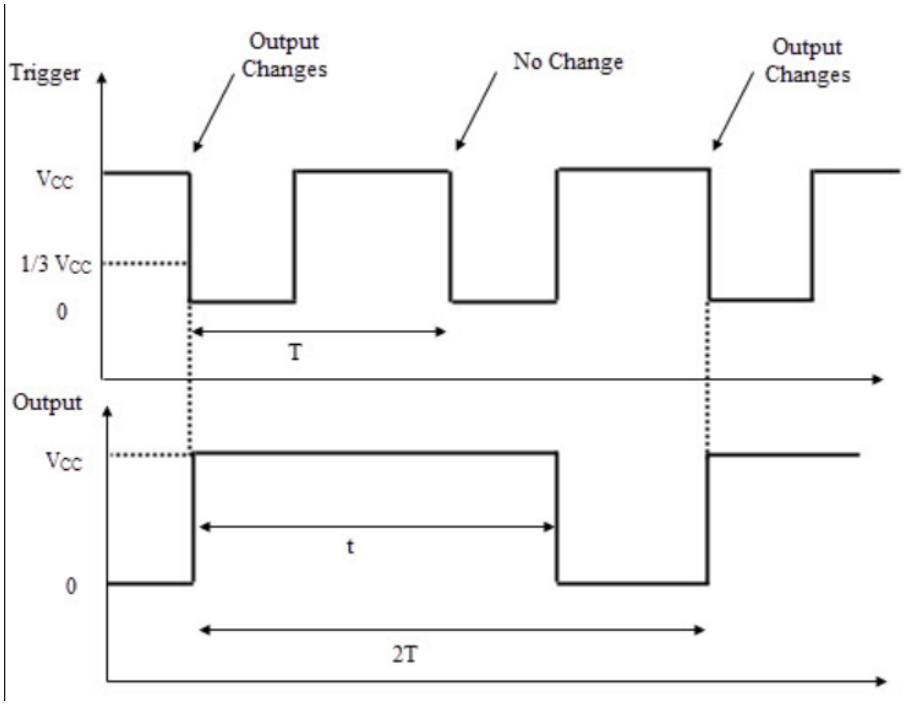


Applications of Monostable Multivibrator

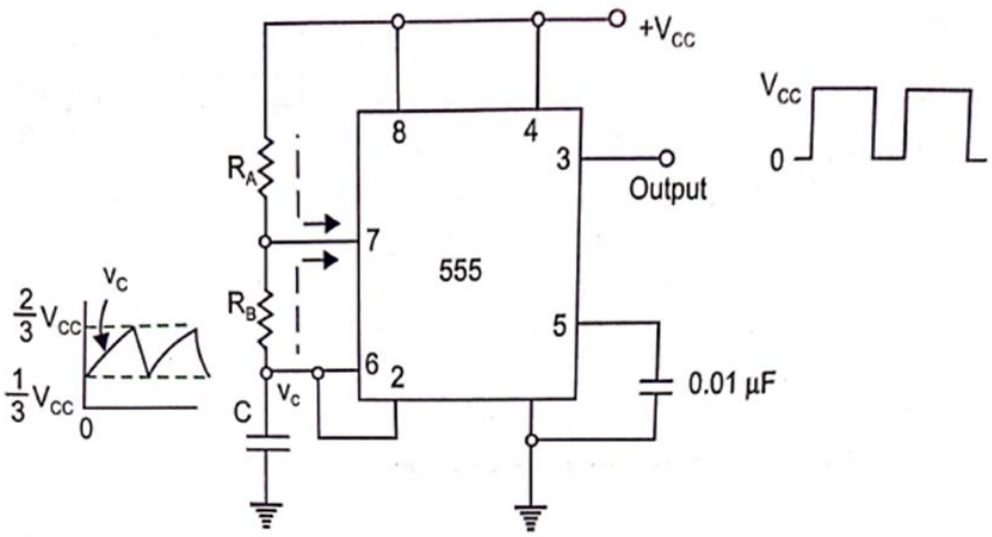
Frequency Divider

When the IC 555 is used as a monostable multivibrator, a positive going rectangular pulse is available at the output when a negative going pulse of short duration is applied at the trigger input. By adjusting the time interval t of the charging or timing circuit the device can be made to work as a Frequency Divider circuit.

If the timing interval t is made slightly larger than the time period of the input pulse (trigger pulse), the device can act as a Divide – by – two circuit. The timing interval can be controlled by appropriately choosing the values of the resistor R and the capacitor C in the timing circuit. The waveforms of the input and output signals corresponding to the divide–by–two circuit are shown below.

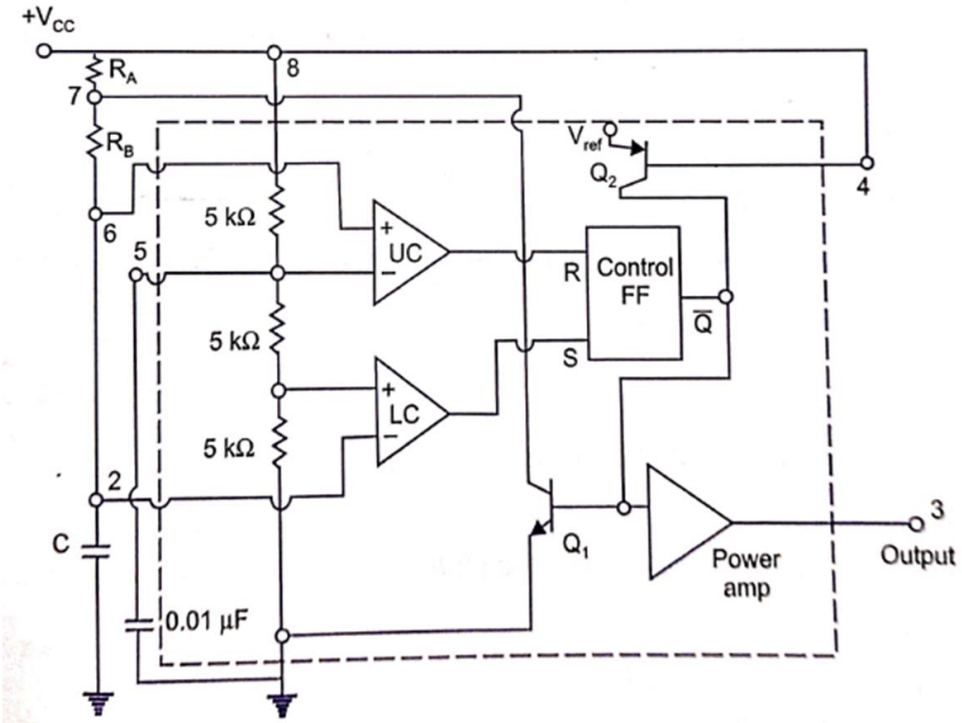


Astable Multivibrator



Astable multivibrator using 555 timer

Astable Multivibrator-working



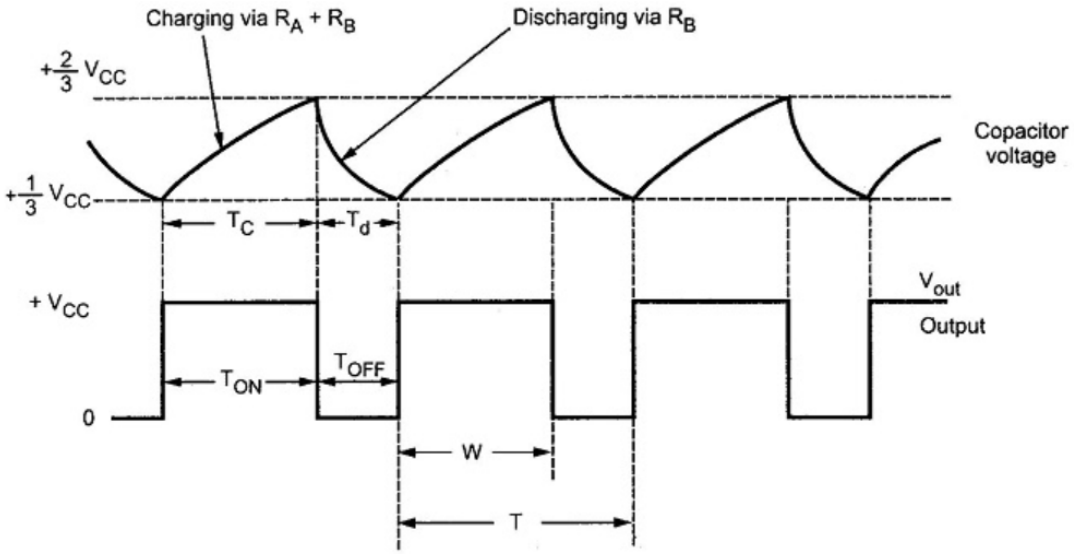
Working of Astable Multivibrator using IC 555:

When the flip-flop is set, Q is high which drives the transistor Q_d in saturation and the capacitor gets discharged. Now the capacitor voltage is nothing but the trigger voltage. So while discharging, when it becomes less than 1/3 V_{CC}, comparator 2 output goes high. This resets the flip-flop hence Q goes low and $\bar{Q}$ goes high.

The low Q makes the transistor off. Thus capacitor starts charging through the resistances R_A, R_B and V_{CC}. The charging path is shown by thick arrows in the Fig. 2.105. As total resistance in the charging path is (R_A + R_B), the charging time constant is (R_A + R_B) C.

Now the capacitor voltage is also a threshold voltage. While charging, capacitor voltage increases i.e. the threshold voltage increases. When it exceeds 2/3 V_{CC}, then the comparator 1 output goes high which sets the flip-flop. The flip-flop output Q becomes high and output at pin 3 i.e. $\bar{Q}$ becomes low. High Q drives transistor Q_d in saturation and capacitor starts discharging through resistance R_B and transistor Q_d. This path is shown by dotted arrows in the Fig. 2.105. Thus the discharging time constant is R_B C. When capacitor voltage becomes less than 1/3 V_{CC}, comparator 2 output goes high, resetting the flip-flop. This cycle repeats.

Thus when capacitor is charging, output is high while when it is discharging the output is low. The output is a rectangular wave. The capacitor voltage is exponentially rising and falling. The waveforms of Astable Multivibrator using 555 Timer IC are shown in the Fig. 2.106



Duty Cycle of Astable Multivibrator:

Generally the charging time constant is greater than the discharging time constant. Hence at the output, the waveform is not symmetric. The high output remains for longer period than low output. The ratio of high output period and low output period is given by a mathematical parameter called **duty cycle. It is defined as the ratio of ON time i.e. high output to the total time of one cycle.** As shown in the Fig. 2.106.

$$W = \text{time for output is high} = T_{ON}$$

$$T = \text{time of one cycle}$$

$$\therefore \quad D = \text{duty cycle} = \frac{W}{T}$$

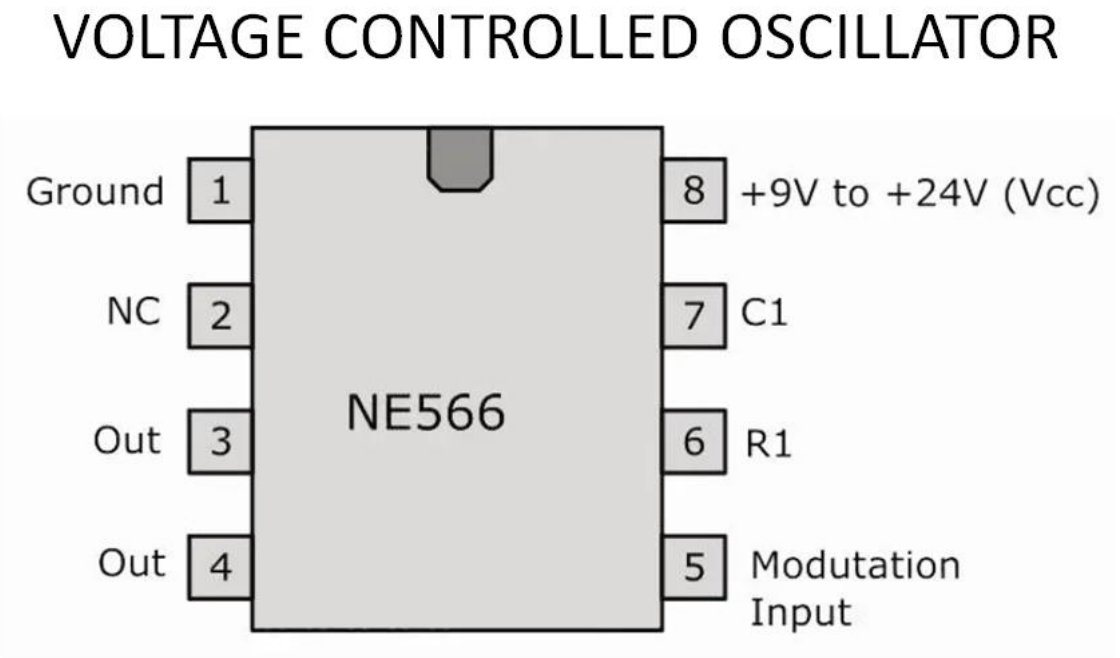
$$\therefore \quad \%\, D = \frac{W}{T} \times 100\ \%$$

Applications of Astable Multivibrator

Square Wave Generation

The duty cycle of an astable multivibrator is always greater than 50%. A square wave is obtained as the output of an astable multivibrator when the duty cycle is 50% exactly. Duty cycle of 50% or anything less than that is not possible with the IC 555 as an astable multivibrator mentioned above. Some modifications are to be made to the circuit.

The modification is to add two diodes. One diode in parallel to the resistor R_2 with cathode connected to the capacitor and another diode in series with the resistor R_2 with anode connected to the capacitor. By adjusting the values of the resistors R_1 and R_2, a duty cycle in the range of 5% to 95% can be obtained including the square wave output. The circuit for square wave generation is shown below.



VCO

A ***Voltage-Controlled Oscillator*** (**VCO**) is a circuit that provides a varying output signal (typically of square-wave or triangular-wave form) whose frequency can be adjusted over a range controlled by ***an externally applied DC voltage.***

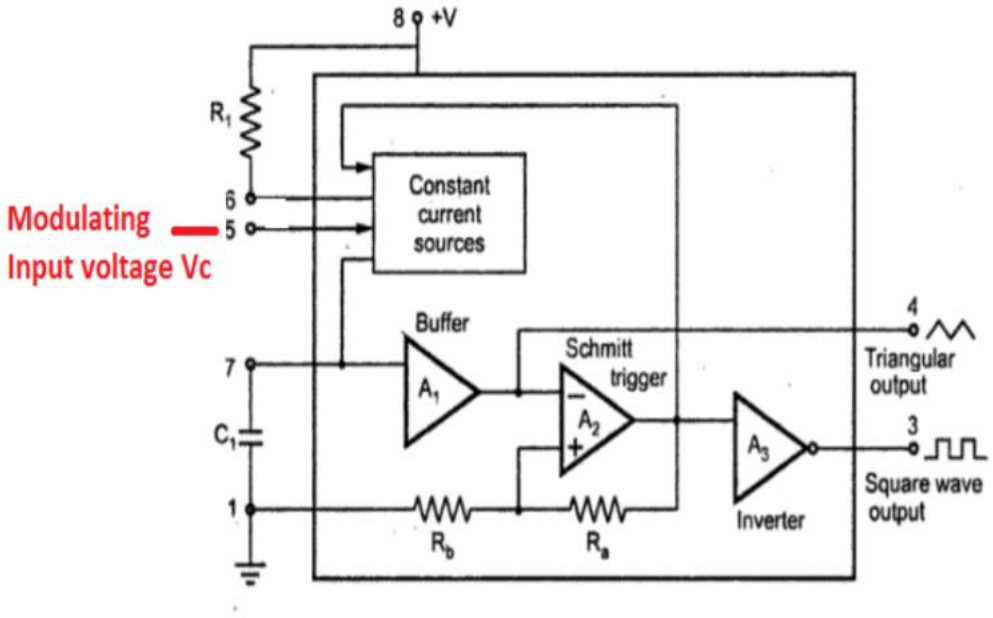
The VCO provides a linear relationship between the applied voltage and the oscillation frequency. The applied voltage is called **control voltage**.

The control of frequency with the help of control voltage is known as **voltage to frequency conversion**. Hence VCO is otherwise known as *Voltage to frequency converter*.

Practically VCO is available in IC form. IC 566 (LM566/SE566) from Signetics is a popular VCO. IC 566 contains circuitry to generate both squarewave and triangular-wave signals whose frequency is set by an external resistor and capacitor and then varied by an applied dc voltage.

IC 566 is an 8 pin IC,

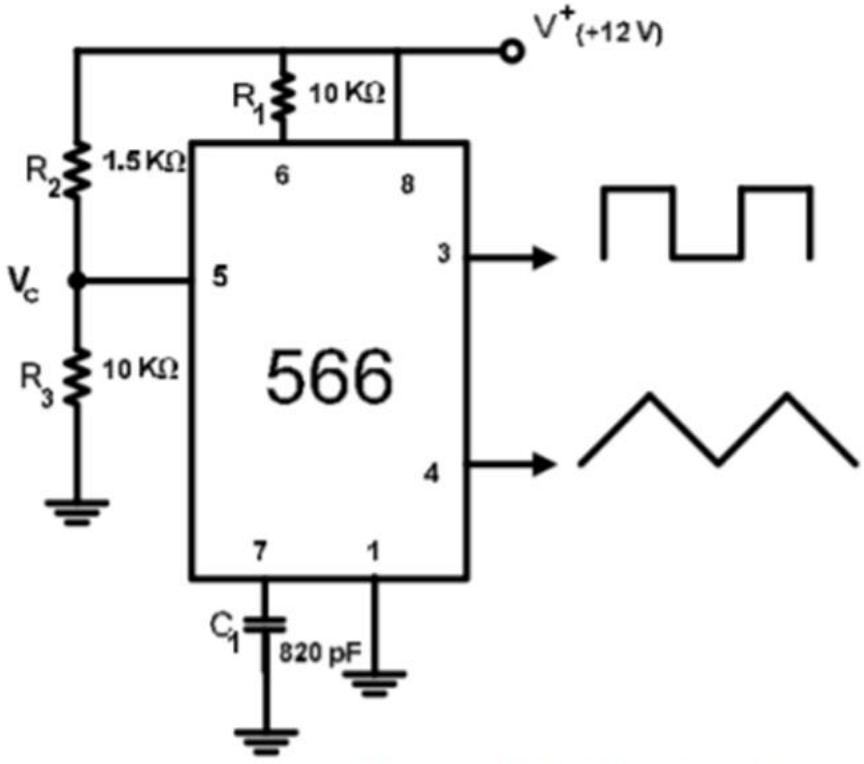
- Two output pins for Square and Triangular outputs.
- The frequency of the Square and Triangular waves are function of the input voltage applied at Pin 5. This input voltage is also called as Modulating Input voltage.
- The Frequency of the output voltage is determined by R1 , C1 and Control Voltage Vc



Block diagram of IC566

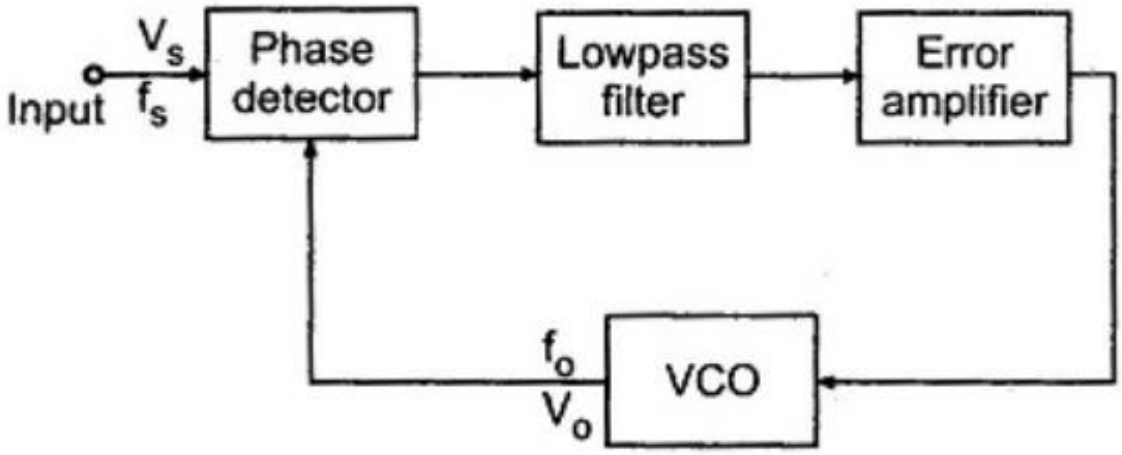
Principle of Operation

- The op-amp A1 is used a buffer.
- The op-amp A2 is used as Schmitt trigger.
- The op-amp A3 is used a an Inverter.
- The Voltage Vc is applied to the modulation input pin which is a control voltage.
- The capacitor C1 is linearly charged or discharged by a constant current source.
- The charging current can be controlled by controlling the voltage Vc at pin 5 or by varying the resistance R1 which is external to the IC.
- The charging and discharging levels are determined by the Schmitt trigger
- The output voltage of Schmitt trigger is designed to swing between +V and 0.5V
- For Ra= Rb, the voltage at non-inverting terminal swings between 0.5(+V) to 0.25(+V).
- Thus the triangular wave is generated due to alternate charging and discharging of the capacitor C1 in linear manner.
- When C1 voltage increases beyond 0.5(+V), the ST output goes low, and the capacitor starts discharging.
- When the voltage becomes less than 0.25(+V), the output of the ST goes high.
- Due to similar current sources used for charging and discharging, the time taken by C1 to charge and discharge is same. This produces exact triangular wave.
- The output of the ST is step response, which is a square wave output.



Connection of 566 VCO unit.

PLL Block Diagram:



It consists of

- Phase detector
- Low pass filter
- Error amplifier
- Voltage Controlled Oscillator (VCO)

The phase detector compares the input frequency f_i with the feedback frequency f_o and generates an output signal which is a function of the difference between the phases of the two input signals. The output signal of the phase detector is a dc voltage. The output of phase detector is applied to low-pass filter to remove high frequency noise from the dc voltage. The output of low pass filter without high frequency noise is often referred to as error voltage or control voltage for VCO.

When control voltage is zero, VCO is in free running mode and its output frequency is called as centre frequency f_o. The non-zero control voltage results in a shift in the VCO frequency from its free-running frequency, f_o to a frequency f, given by

$$f = f_o + K_V V_C$$

where K_V is the voltage to frequency transfer coefficient of the VCO. The error or control voltage applied as an input to the VCO, forces the VCO to change its output frequency in the direction that reduces the difference between the input frequency and the output frequency of VCO.

This action, commonly known as capturing, continues till the output frequency of VCO is same as the input signal frequency. Once the two frequencies are same, the circuit is said to be locked. In locked condition, phase detector generates a constant dc level which is required to shift the output frequency of VCO from centre frequency to the input frequency. Once locked, PLL tracks the frequency changes of the input signal. Thus, a Phase Locked Loop Working goes through three states. : **free running**, **capture** and **phase lock**.

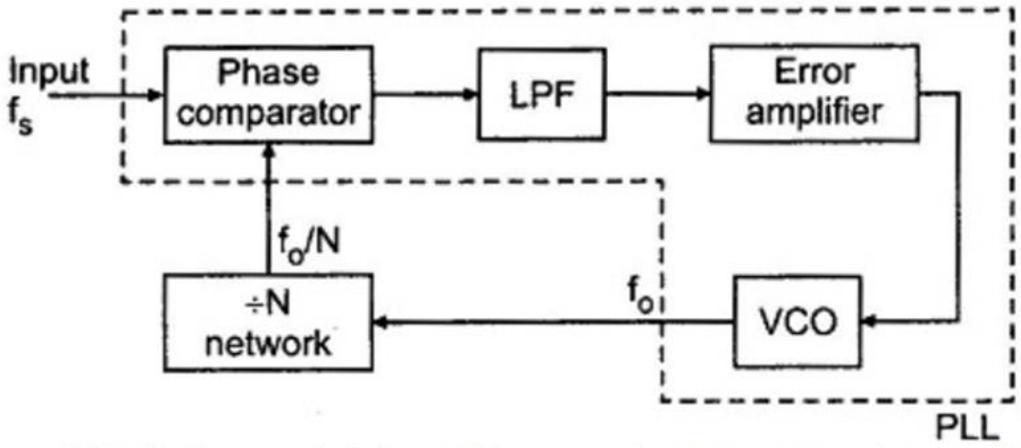
Lock Range:

When PLL is in lock, it can track frequency changes in the incoming signal. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the **lock range** or **tracking range** of the PLL. It is usually expressed as a percentage of f_o, the VCO frequency.

Capture Range:

The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. It is also expressed as a percentage of f_o.

Frequency Multiplier using PLL 565:



Here , a divide by N network is inserted between the VCO output (pin 4) and the phase comparator input (pin 5). Since the output of the divider is locked to the input frequency f_i, the VCO is actually running at a multiple of the input frequency. Therefore, in the locked state, the VCO output frequency f_o is given by,

$$f_o = Nf_i$$

By selecting proper divider by N network, we can obtain desired multiplication.

IC Voltage Regulators

- Voltage regulator: is a circuit that supplies constant voltage regardless of changes in the load current.
- Advantages of IC voltage regulator:

inexpensive,versatile,provides current /voltage boosting, internal short circuit current limiting, thermal shutdown, floating operation for high voltage applications.

Classification of IC voltage regulators:

- There are basically two kinds of IC voltage regulators:
  - Multi-pin type, e.g. LM723C
  - 3-pin type, e.g. 78/79XX
- Multi-pin regulators are less popular but they provide the greatest flexibility and produce the highest quality voltage regulation
- 3-pin types make regulator circuit design simple

• Types of IC voltage regulators:

- Fixed output voltage regulators: positive fixed output regulator(78XX series) and negative fixed output regulator(79XX series)
- Adjustable output voltage regulators: positive (LM317) and negative(LM337)
- Switching regulators: motorola 's MC1723
- NOTE: MC1723 is a general purpose regulator ;it can be used in many ways as a fixed positive or negative output voltage regulator, variable output voltage regulator or as a switching regulator.Due to its flexibility it has become as a standard type in the electronics industry.

Need for regulation

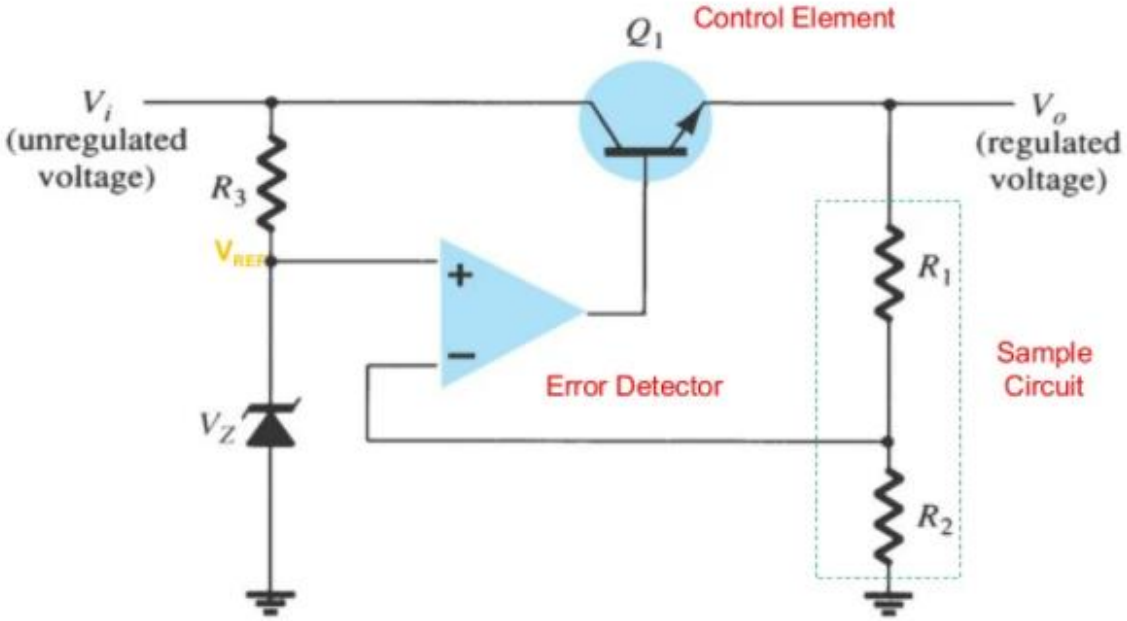
- Without stable potentials, circuit performance degrades and if the variations are large enough the components may get destroyed.
- In order to avoid this regulation is used

Voltage Regulation

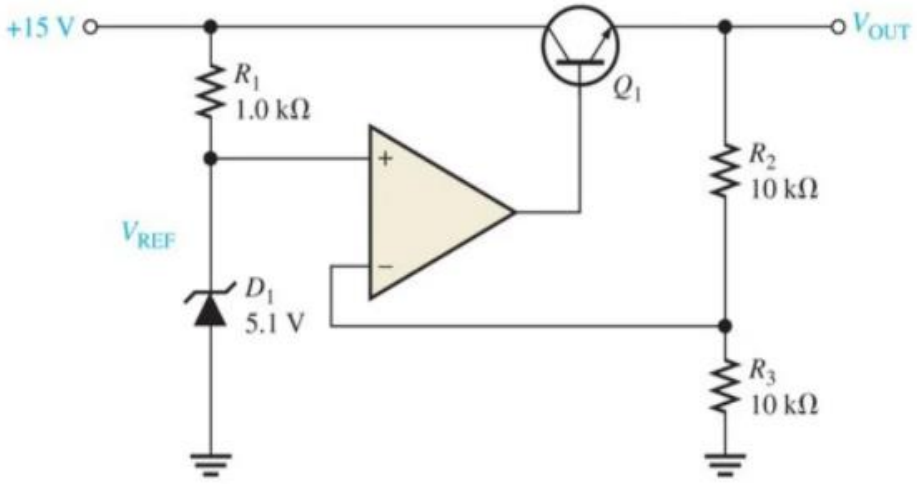
- Two basic categories of voltage regulation are:
  - line regulation
  - load regulation

- The purpose of **line regulation** is to maintain a nearly constant output voltage when the **input voltage** varies.
- The purpose of **load regulation** is to maintain a nearly constant output voltage when the **load** varies

Op-Amp Series Regulator



Example



Op-Amp Series Regulator

- The resistor R_1 and R_2 sense a change in the output voltage and provide a feedback voltage.
- The error detector compares the feedback voltage with a Zener diode reference voltage.
- The resulting difference voltage causes the transistor Q_1 controls the conduction to compensate the variation of the output voltage.
- The output voltage will be maintained at a constant value of:

$$V_o = \left(1 + \frac{R_1}{R_2}\right) V_Z$$

Fixed voltage regulator

A **fixed voltage regulator** produces a fixed DC output voltage, which is either positive or negative. In other words, some fixed voltage regulators produce positive fixed DC voltage values, while others produce negative fixed DC voltage values.

78xx voltage regulator ICs produce positive fixed DC voltage values, whereas, 79xx voltage regulator ICs produce negative fixed DC voltage values.

The following points are to be noted while working with **78xx** and **79xx** voltage regulator ICs −

- "xx" corresponds to a two-digit number and represents the amount (magnitude) of voltage that voltage regulator IC produces.
- Both 78xx and 79xx voltage regulator ICs have **3 pins** each and the third pin is used for collecting the output from them.

The function of a **voltage regulator** is to maintain a constant DC voltage at the output irrespective of voltage fluctuations at the input and (or) variations in the load current. In other words, voltage regulator produces a regulated DC output voltage.

Voltage regulators are also available in Integrated Circuits (IC) forms. These are called as **voltage regulator ICs**.

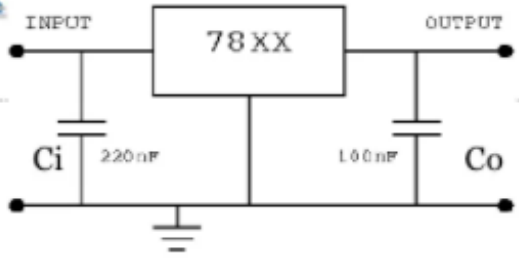
Types of Voltage Regulators

There are **two types** of voltage regulators −

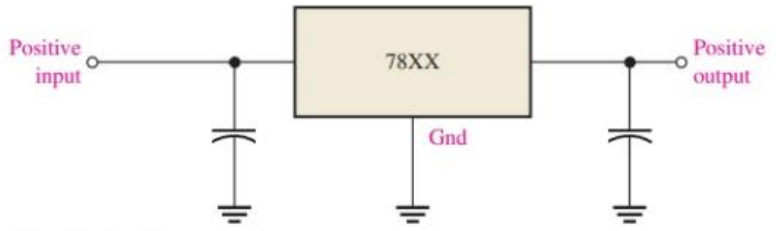
- Fixed voltage regulator
- Adjustable voltage regulator

FIXED VOLTAGE REGULATOR

a)positive voltage regulator



- The 78XX voltage regulators
- Fig shows the connection diagram of 78XX series
- Proper operation requires a common ground between the input and output voltages.
- The difference between the input and output voltages(V_{in}- V_{out}) called dropout voltage must be 2V even during low point in the input ripple voltage.
- Capacitor C_i, is required if the regulator is located an appreciable distance from a power supply filter. Even though C_o is not required, it may be used to improve the transient response of the regulator.



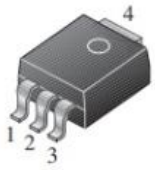
(a) Standard configuration

Type number	Output voltage
7805	+5.0 V
7806	+6.0 V
7808	+8.0 V
7809	+9.0 V
7812	+12.0 V
7815	+15.0 V
7818	+18.0 V
7824	+24.0 V

(b) The 78XX series

Pin 1. Input
2. Ground
3. Output

Heatsink surface connected to Pin 2.

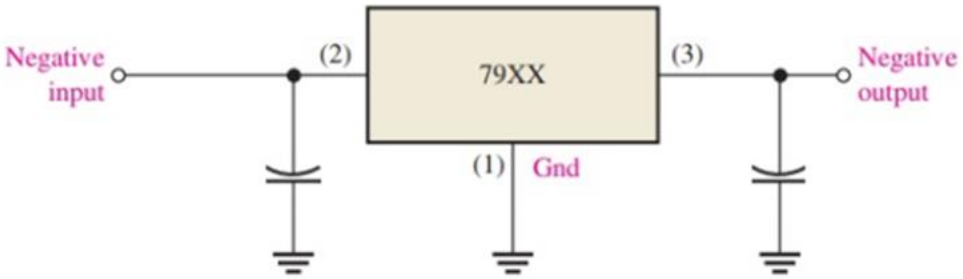


Heatsink surface (shown as terminal 4 in case outline drawing) is connected to Pin 2.

(c) Typical packages

78XX series three-terminal fixed positive voltage regulators

Fixed Negative Linear Voltage Regulators



Type number	Output voltage
7905	–5.0 V
7905.2	–5.2 V
7906	–6.0 V
7908	–8.0 V
7912	–12.0 V
7915	–15.0 V
7918	–18.0 V
7924	–24.0 V

(b) The 79XX series

Adjustable voltage regulator

An adjustable voltage regulator produces a DC output voltage, which can be adjusted to any other value of certain voltage range. Hence, adjustable voltage regulator is also called as a **variable voltage regulator**.

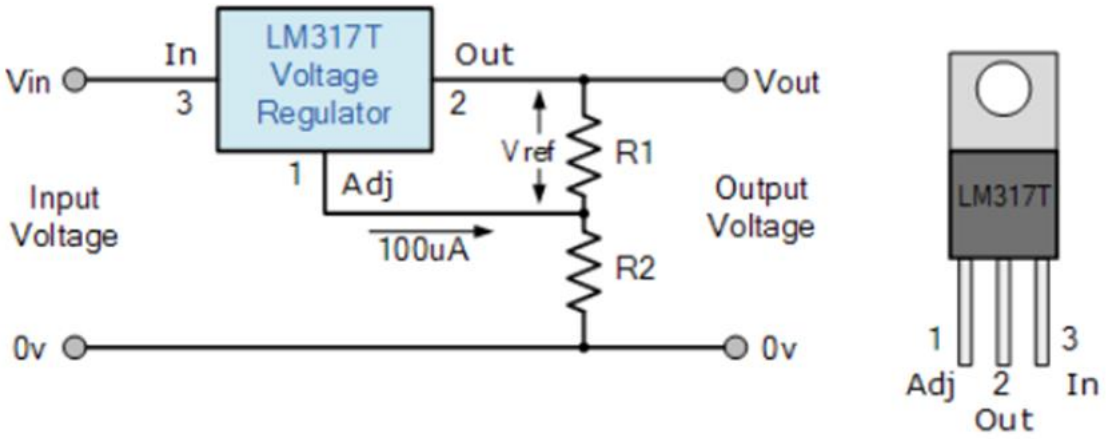
The DC output voltage value of an adjustable voltage regulator can be either positive or negative.

LM317 voltage regulator IC

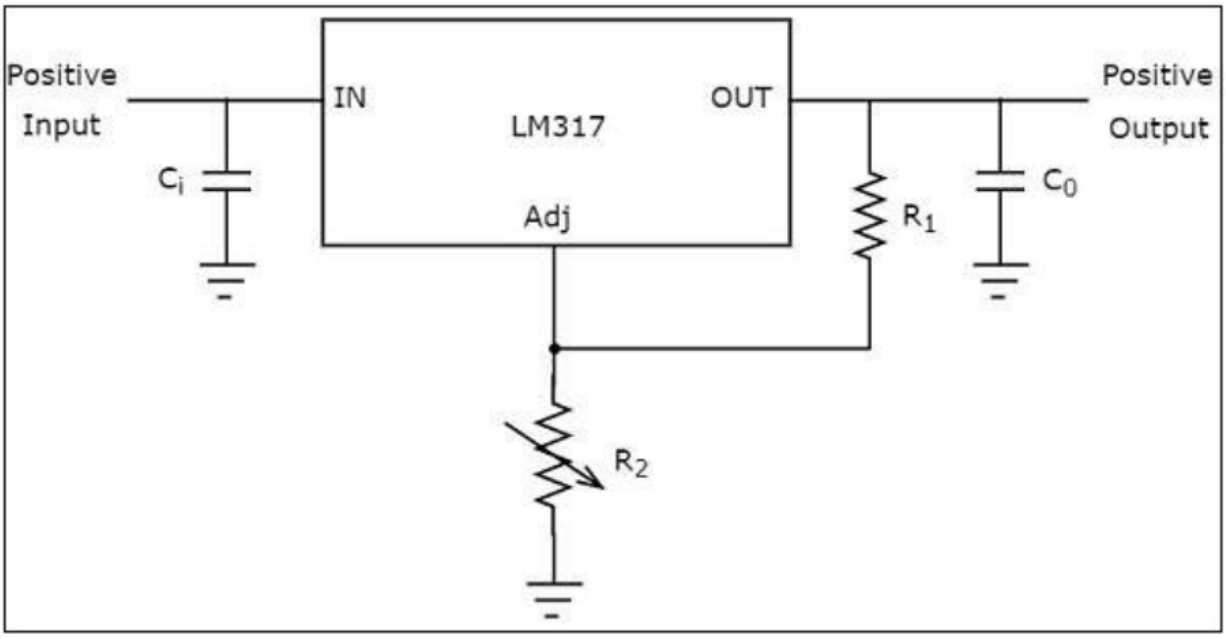
LM317 voltage regulator IC can be used for producing a desired positive fixed DC voltage value of the available voltage range.

LM317 voltage regulator IC has 3 pins. The first pin is used for adjusting the output voltage, second pin is used for collecting the output and third pin is used for connecting the input.

The adjustable pin (terminal) is provided with a variable resistor which lets the output to vary between a wide range.



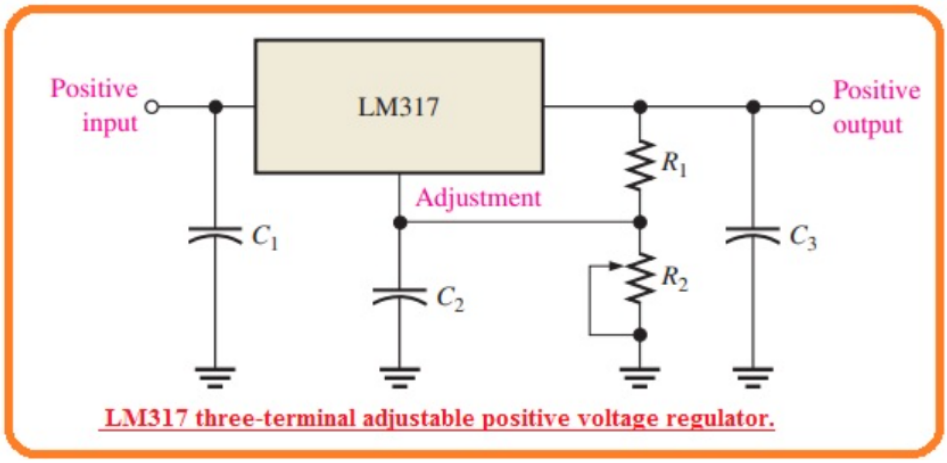
The LM317T is an adjustable 3-terminal positive voltage regulator capable of supplying different DC voltage outputs other than the fixed voltage power supply of +5 or +12 volts, or as a variable output voltage from a few volts up to some maximum value all with currents of about 1.5 amperes.



The above figure shows an unregulated power supply driving a LM 317 voltage regulator IC, which is commonly used. This IC can supply a load current of 1.5A over an adjustable output range of 1.25 V to 37 V.

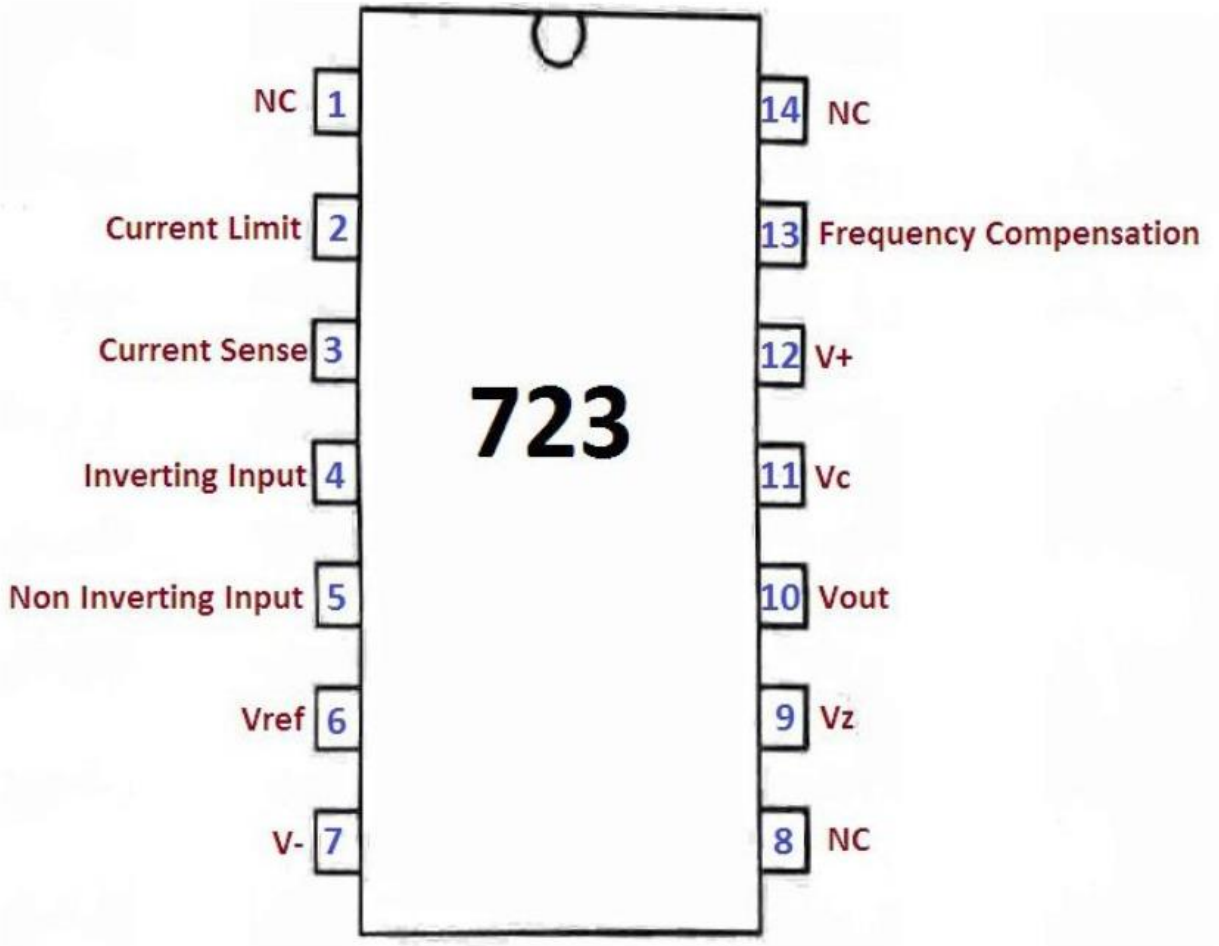
Adjustable Positive Linear Voltage Regulators

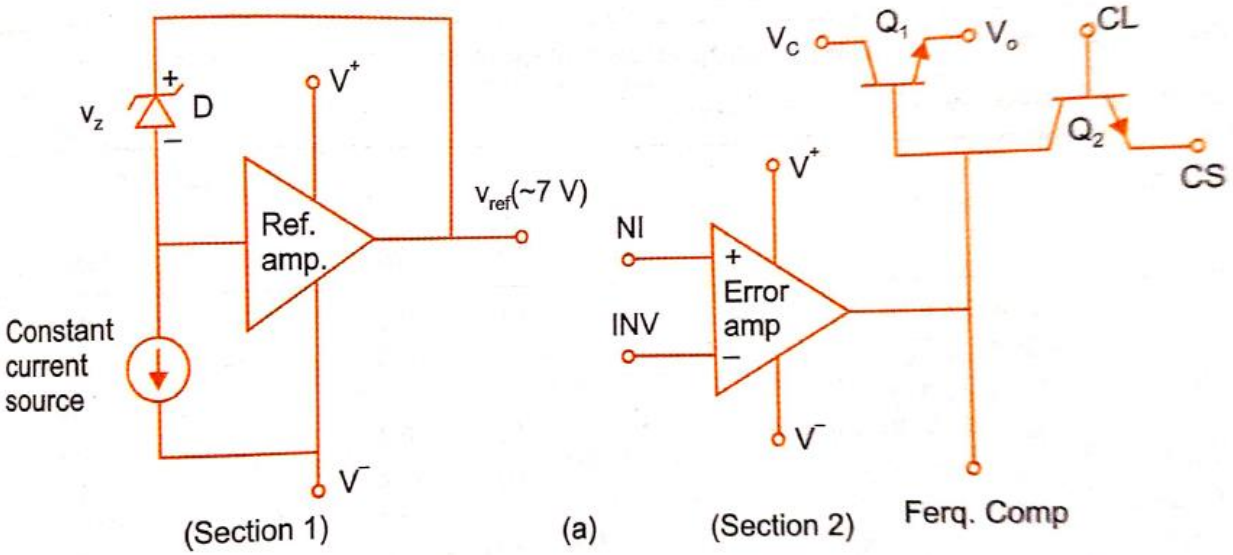
- The LM317 is a common example of 3 terminal positive regulators having variable output capacity.
- The basic arrangement is can be seen in the below figure.



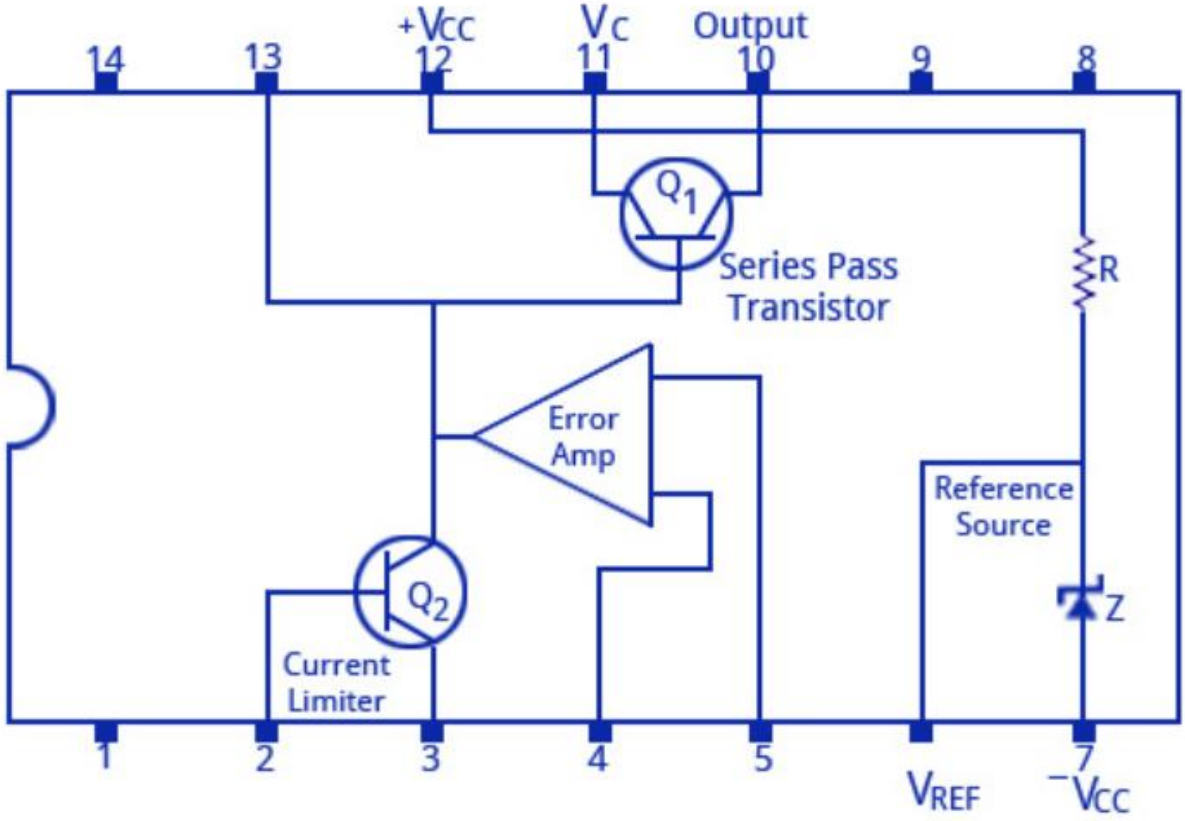
LM317 three-terminal adjustable positive voltage regulator.

- The capacitor are used for decoupling and has not any effect on the dc operation.
- Note that there is an input-output and variable terminal.
- The exterior fixed-resistance and outer variable resistance offer the output voltage variance or adjustment.
- The value of VOut can be changed from 1.2 volts to thirty-seven volts according to the value of resistance.
- The LM317 can offer large then the 1.5 amperes output current to the output.
- LM317 is functioning like a floating regulator since the adjustment terminal is not linked with the ground but floats the value of voltage about the resistance R2.
- It permits the output voltage to be larger than the fixed voltage regulator.





IC 723 Voltage Regulator Circuit



IC voltage regulators, the 723 Voltage Regulator IC. The functional diagram of the voltage regulator is shown below. It consists of a voltage reference source (Pin 6), an error amplifier with its inverting input on pin 4 and non-inverting input on pin 5, a series pass transistor (pins 10 and 11), and a current limiting transistor on pins 2 and 3. The device can be set to work as both posistive and negaive voltage regulators with an output voltage ranging from 2 V to 37 V, and output current levels upto 150 m A. The maximum supply voltage is 40 V, and the line and load regulations are each specified as 0.01%.

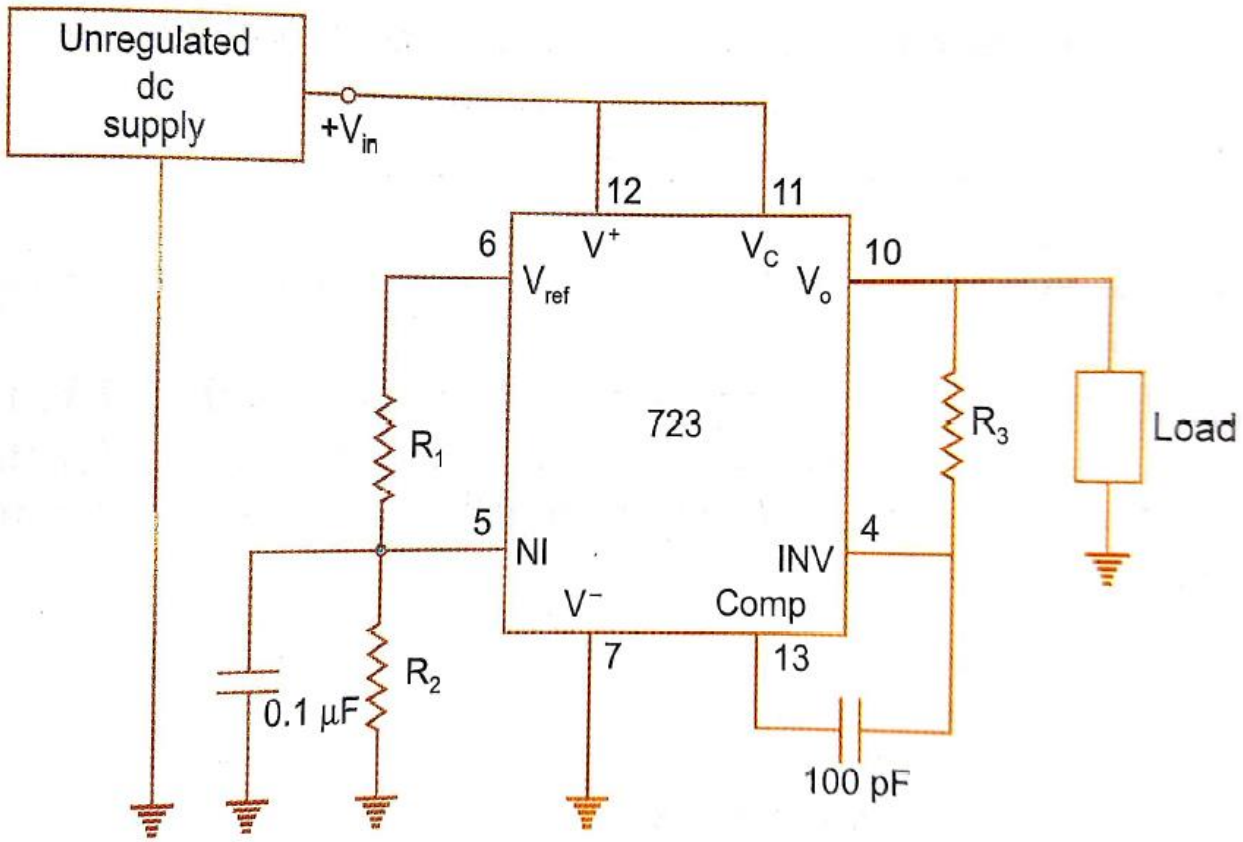


Fig. 6.8 (a) A low voltage regulator using 723 IC

- R_1 & R_2 from a potential divider between V_{ref} & Gnd.
- The Voltage across R_2 is connected to the Non – inverting terminal of the regulator I_C $V_{non\text{-}inv} = R_2/(R_1+R_2)$ Vref
- Gain of the internal error amplifier is large

$V_{non\text{-}inv} = V_{in}$

- Therefore the Vo is connected to the Inverting terminal through R_3 & R_{SC} must also be equal to $V_{non\text{-}inv}$

$V_o = V_{non\text{-}inv} = R_2/(R_1+R_2)\, V_{ref}$

R_1 & R_2 can be in the range of 1 KΩ to 10KΩ & value of R3 is given by

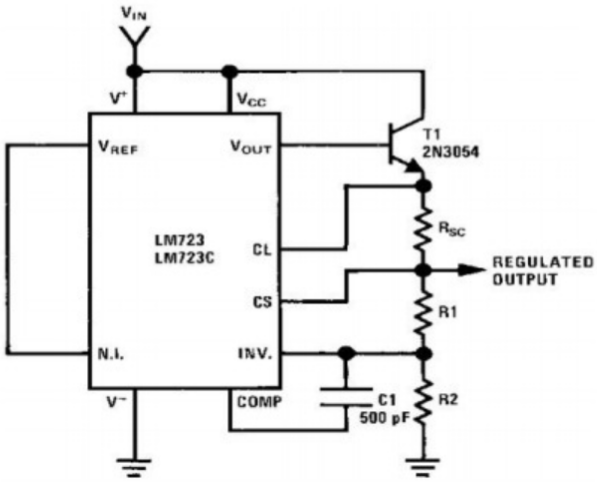
$R_3 = R_1 \text{ll } R_2 = R_1R_2/(R_1+R_2)$

Rsc (current sensing resistor) is connected between Cs & CL. The voltage drop across Rsc is proportional to the IL.

- This resistor supplies the output voltage in the range of 2 to 7 volts, but the load current can be higher than 150mA.
- The current sourcing capacity is increased by including a transistor Q in the circuit.
- The output voltage , Vo $= R_2/(R_1+R_2)\, V_{ref}$

IC723 as a HIGH voltage HIGH Current:

- An external transistor Q is added in the circuit for high voltage low current regulator to improve its current sourcing capacity.



- For this circuit the output voltage varies between 7 & 37V.
- Transistor Q increase the current sourcing capacity thus IL (MAX) is greater than 150mA.
- The output voltage Vo is given by ,

V_0= Vo = $[1+R_1/R_2]\ V_{in}$

Rsc =0.6/Ilimit

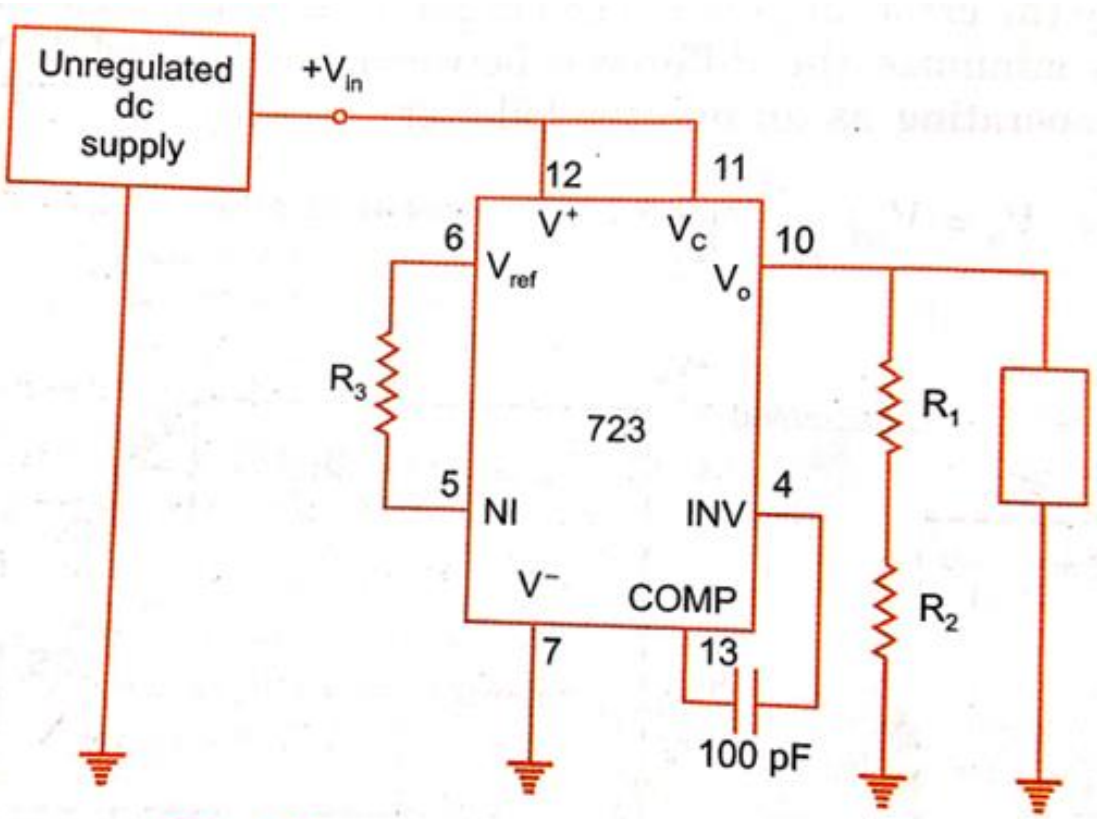


Fig. 6.8 (c) Basic high voltage 723 regulator

- For this circuit the output voltage varies between 7 & 37V.
- Transistor Q increase the current sourcing capacity thus IL (MAX) is greater than 150mA.
- The output voltage Vo is given by ,

V_0= Vo = [1+R_1/R_2] V_{in}

Rsc =0.6/Ilimit

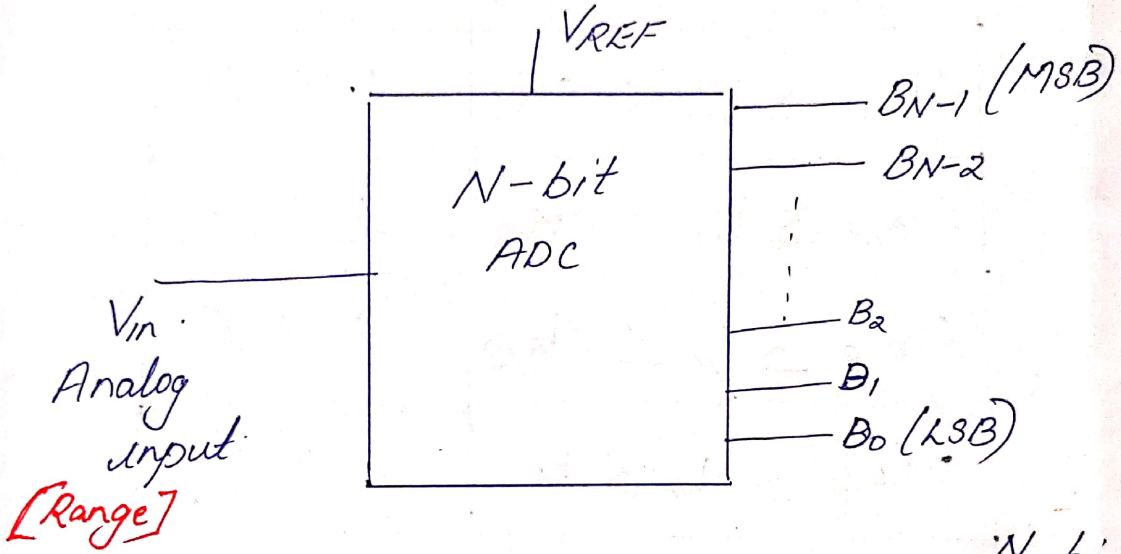
The important features of IC 723 regulators are

- It has small in size and lower in cost.
- It operates in positive or negative supply operation.
- It has choice of supply voltage.
- Wide variety of applications such as series, shunt, switching and floating regulators.
- Relative simplicity with power supply can be designed.
- Low standby current gain.
- Very low temperature drift and high ripple rejection.
- Built in fold back current limiting.
- Input voltage is maximum 40 V.
- Output voltage adjustable from 2 V to 37 V.
- Output current upto 150 mA without external pass transistor.
- Load and line regulations of 0.03%.

MODULE-VI

Analog to Digital Converter's [A/D Converters]

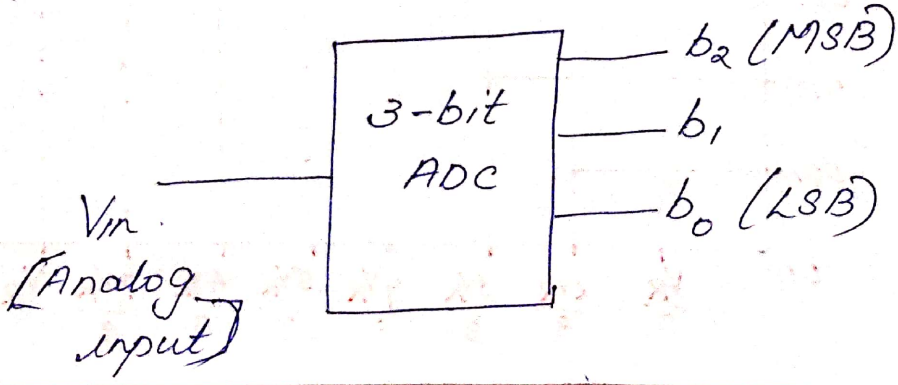
An A/D Converter does the inverse function of a D/A converter. It converts an analog signal into its equivalent N-bit binary coded digital output signal.



For N bit ADC, there are 2^N binary output combinations. The A/D Conversion process divides the analog input V_{IN} into 2^N intervals.

Eg: If the input analog voltage range is 0 to 5V, then $V_{FS} = 5V$, where V_{FS} is the full-scale analog voltage.

Eg:- 3-bit ADC.

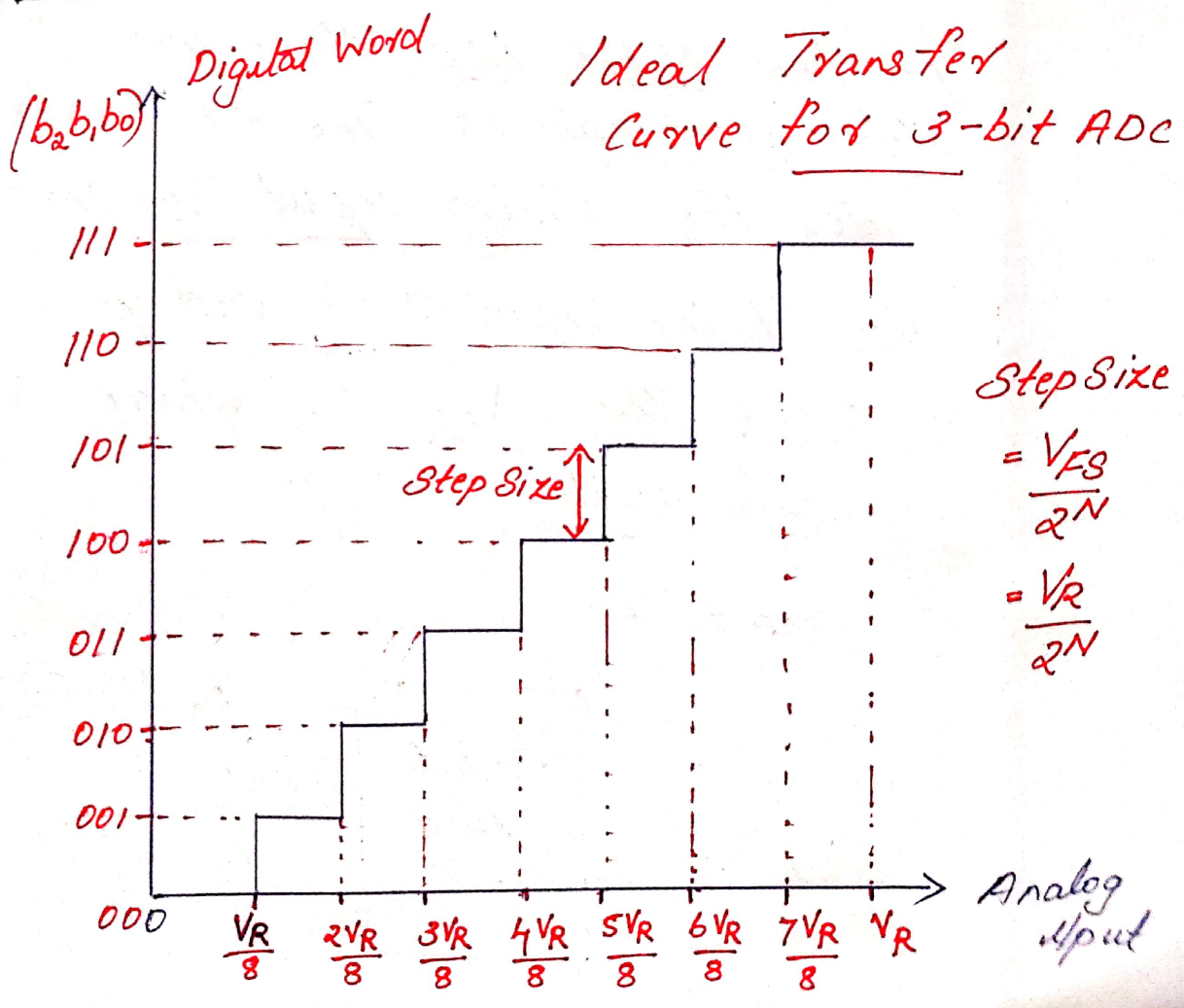


Truth table for 3-bit ADC ($V_{FS} = V_R$)

Analog Input Voltage	Digital O/p b_2 b_1 b_0
$0 \le V_{in} \le V_R/8$	0 0 0
$V_R/8 \le V_{in} \le 2V_R/8$	0 0 1
$2V_R/8 \le V_{in} \le 3V_R/8$	0 1 0
$3V_R/8 \le V_{in} \le 4V_R/8$	0 1 1
$4V_R/8 \le V_{in} \le 5V_R/8$	1 0 0
$5V_R/8 \le V_{in} \le 6V_R/8$	1 0 1
$6V_R/8 \le V_{in} \le 7V_R/8$	1 1 0
$7V_R/8 \le V_{in} \le V_R$	1 1 1

2^N quantization levels

Ideal Transfer Curve for 3-bit ADC



Step Size $= \frac{V_{FS}}{2^N} = \frac{V_R}{2^N}$

For a 8 bit ADC, $V_{FS} = 1V$

$$\text{Then Step size} = \frac{V_R}{2^N} = \frac{V_{FS}}{2^N} = \frac{1V}{28} = 3.9mV$$

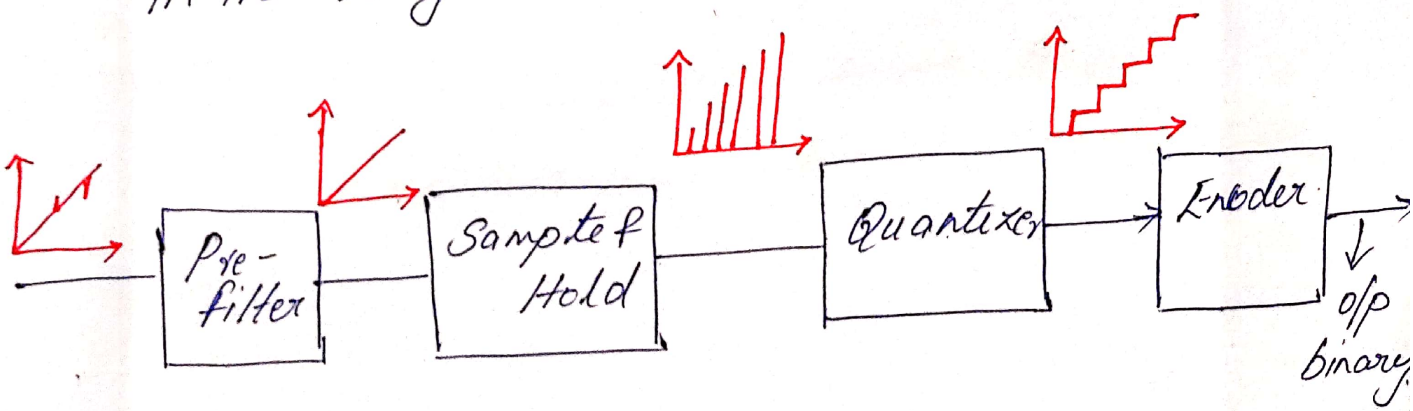
3.9mV is the finest minimum change in the signal which is accepted for conversion.

For a 16 bit ADC, $V_{FS} = 1V$

$$\text{Step size} = \frac{V_R}{2^N} = \frac{V_{FS}}{2^N} = \frac{1V}{2^{16}} = 15.26\mu V$$

Output binary should change to adjacent code for a minimum change of 15.26μV.

So As the number of bits increases, the step size reduces, so the ADC should be highly precise and accurate to detect these changes in the range of microvolts.



General block diagram of a A/D Converter.

SPECIFICATIONS OF A/D CONVERTER.

1. Resolution

The resolution refers to the finest minimum change in the signal which is accepted for conversion and it is decided with respect to the number of bits.

$$\text{Resolution} = \frac{1}{2^N}$$, N is the number of digital output word bits.

The ratio of full-scale input voltage range V_{FS} to the 2^N gives the minimum change of input voltage that can cause a change of 1LSB at the output

$$\Delta V_{in} \text{ for 1LSB (step size)} = \frac{V_{FS}}{2^N} = \frac{V_R}{2^N}$$

The maximum full-scale input voltage which will cause the output to be all logic 1s is 1LSB less than the full-scale voltage range.

$$V_{iFS} = V_{FS} - 1LSB$$

V_{iFS} = maximum input voltage which can cause all 1s at the output.

2. Quantization Error,

When the digital numbers are converted back to analog voltage by a D/A converter,

the output will be a staircase waveform

eg: the digital output is 011, for input voltage range $\frac{3V_R}{8} \leq V_{in} \leq \frac{4V_R}{8}$

When 011, is applied to DAC, $\frac{3V_R}{8}$ is obtained as output. Therefore, there is an uncertainty about the exact value of V_{in} when the output is 011. This error is called quantization error. Its value is $\pm \frac{1}{2}$ LSB.

3. Conversion time

The time required for an A/D converter to convert an analog input value into its equivalent digital value.

4. Analog Error

Analog error in an A/D converter is mainly due to variations in the dc switching point of the comparator. The variations in switching are mainly due to offset, gain & linearity error of op-amp used in comparator. Another source of analog error are resistors used in the circuit.

5. Linearity Error

It is defined as a measure of the variation in voltage step size. This indicates

the difference between the transitions for a minimum step of input voltage range.

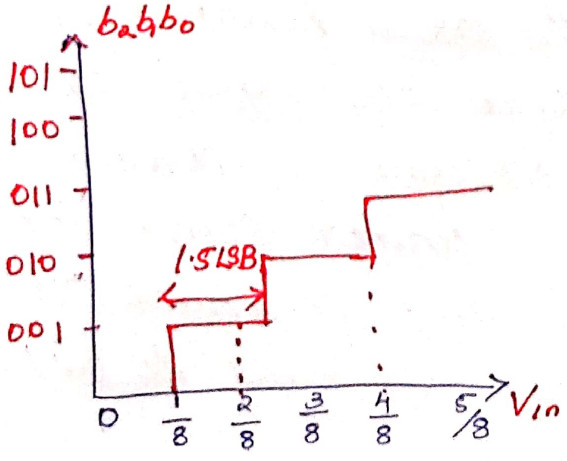
6. Differential non-linearity (DNL)

The analog input levels that trigger any two successive output codes should differ by 1LSB for A/D converter. Any deviation from 1LSB value is defined as DNL error.

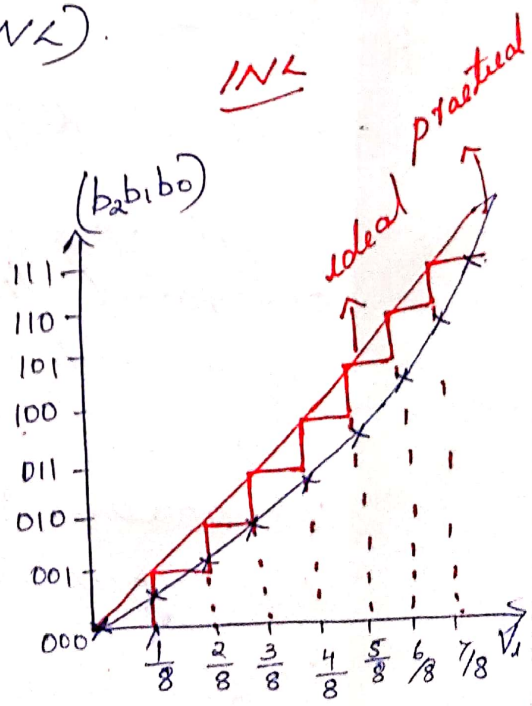
7. Integral non-linearity (INL)

The maximum deviation of the code centre line from the straight line passing through the end points of the ideal characteristics is called Integral Non-linearity error. (INL).

DNL



INL



DNL = 1·5LSB − 1LSB

= 0·5LSB

CLASSIFICATION OF A/D CONVERTERS

1) Type-I

(a) Programmed A/D Converters.

In programmed ADC, the conversion is made in a fixed number of steps, with equal time intervals

eg:- Successive approximation

(b) Non-programmed A/D Converter

It may require a sequence of steps initially and the time interval of the sequence of steps depends only on the response time of the conversion circuitry.

eg:- Integrating type ADC

2) Type-II

(a) Closed-loop or Feedback type A/D.

In closed loop, the analog voltage generated internally as a function of digital input is fed back to one input of the comparator. This voltage is compared with the analog voltage under conversion. When the input voltage and feedback voltages are equal, the conversion is said to be complete.

All D/A converter based A/D converters belong to this category.

(b) Open-loop type A/D Converters.

In open-loop comparator's, a direct comparison is made between the analog input voltage and a set of reference analog voltages.

eg:- Flash type A/D Converters.

3) Type-III

(a) Direct-type A/D Converters.

Direct-type compare a given analog signal with an internally generated equivalent analog signal.

eg:- Flash-type, Counter-type, Successive Approximation type.

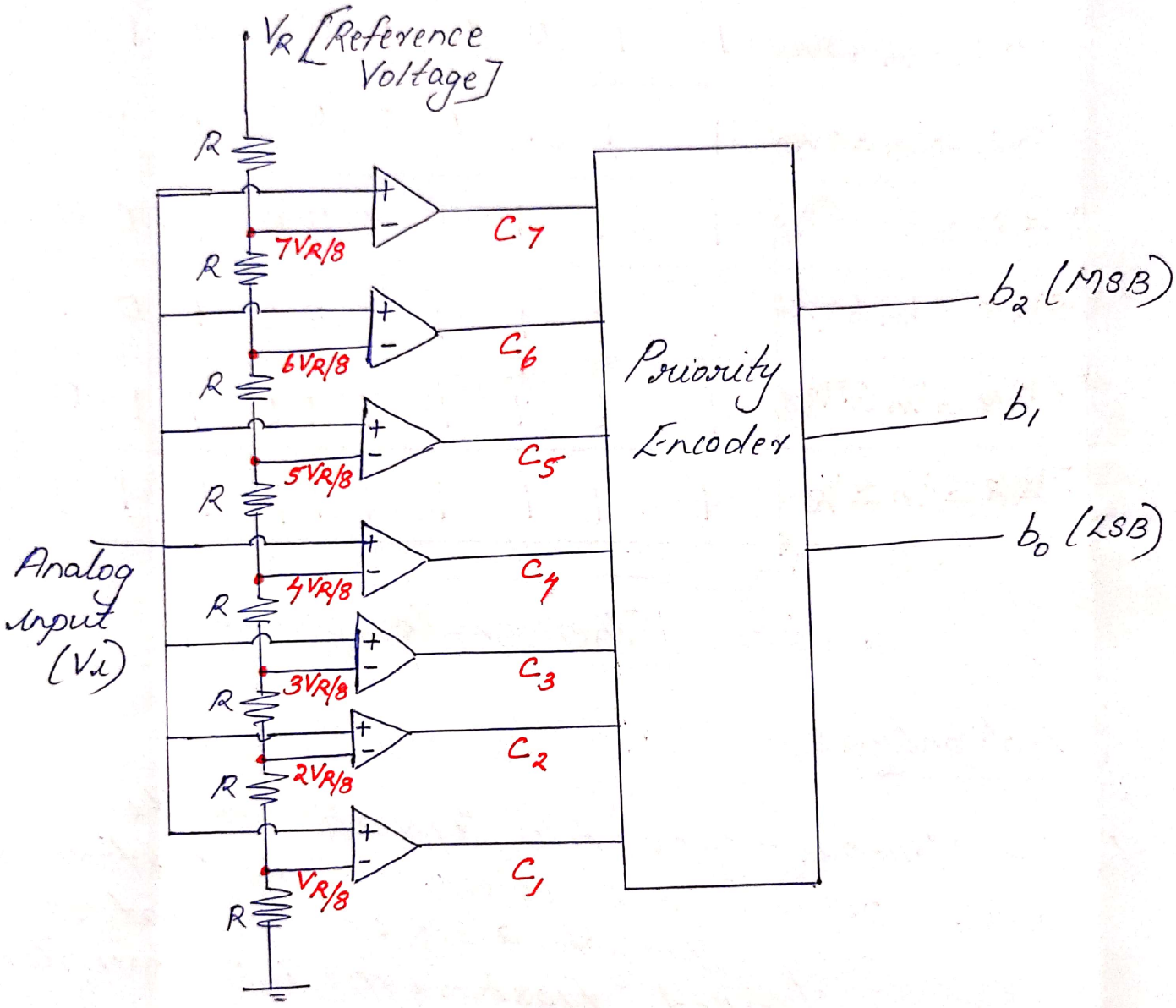
(b) Integrating type A/D Converter.

It uses either a reference voltage or integrates the signal during the conversion process. Suitable only for low frequency signals.

eg:- Single slope ADC
Dual slope ADC

1. Flash Type (A/D Converters)

A 3-bit ADC can be constructed using seven (2^3-1) comparators.



2^3 Resistors & 2^3-1 Comparators for a 3-bit ADC

In general for an N-bit DAC,

2^N Resistors & 2^N-1 comparators are used.

Since priority encoder is used, highest priority is for C_7 and the priority order is

$C_7, C_6, C_5, C_4, C_3, C_2, C_1, C_0$

Truth table:

Analog Input Voltage (V_{in})	C_1	C_2	C_3	C_4	C_5	C_6	C_7	b_2	b_1	b_0
$0 \le V_{in} \le V_R/8$	0	0	0	0	0	0	0	0	0	0
$V_R/8 \le V_{in} \le 2V_R/8$	1	0	0	0	0	0	0	0	0	1
$2V_R/8 \le V_{in} \le 3V_R/8$	1	1	0	0	0	0	0	0	1	0
$3V_R/8 \le V_{in} \le 4V_R/8$	1	1	1	0	0	0	0	0	1	1
$4V_R/8 \le V_{in} \le 5V_R/8$	1	1	1	1	0	0	0	1	0	0
$5V_R/8 \le V_{in} \le 6V_R/8$	1	1	1	1	1	0	0	1	0	1
$6V_R/8 \le V_{in} \le 7V_R/8$	1	1	1	1	1	1	0	1	1	0
$7V_R/8 \le V_{in} \le V_R$	1	1	1	1	1	1	1	1	1	1

Thermometer coding

Advantages:

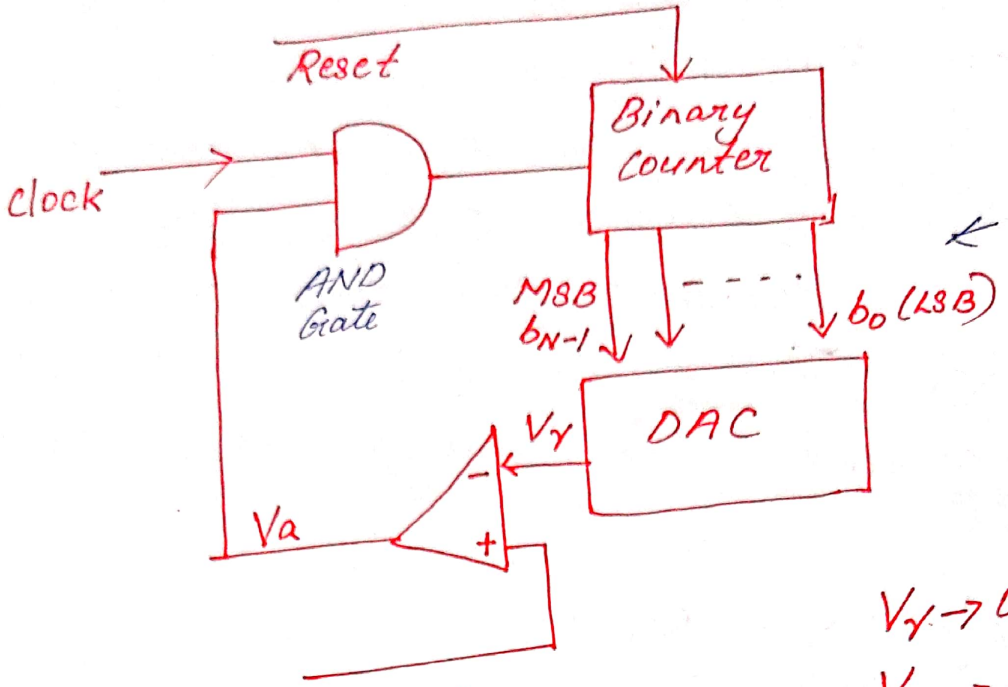
1. Simultaneous-type A/D converter is the fastest because A/D conversion is performed simultaneously through a set of comparators. Hence it is called flash-type A/D converter. Typical conversion time is 100ns.
2. The construction is simple and easier to design.

Disadvantages

(N bits → $2^N - 1$ Comparators)

As the number of bit increases, the number of comparators also increases. Hence the circuit will become bulky and consume more power

2. Counter type A/D Converter.



$V_r \rightarrow$ O/p of DAC

$V_{in} \rightarrow$ Analog i/p

Comparator Action: If $V_{in} > V_r$, $V_a \rightarrow$ High

$V_{in} < V_r$, $V_a \rightarrow$ Low

Working

The n-bit binary counter is initially set to 0 by the Reset switch. Therefore the digital output is 'zero' and the analog output voltage of DAC is 'zero'.

When the Reset signal is released, the clock pulses gated through the AND gate are counted by the binary counter. The D/A converter converts the digital output to an analog voltage (V_r) and supplies it as the inverting input to the comparator. The output of the comparator enables the AND gate to pass the clock.

The counting will continue until the reference voltage V_r equals and just rises more than V_i. The counting stops at the instance $V_r > V_i$ and at that instant the comparator output becomes LOW and this disables the AND gate from passing the clock. The digital output of the counter represents the analog input voltage.

Conversion time.

In this A/D converter, the counter advances by one count for every clock pulse and therefore the clock speed decides the conversion time.

eg:- For a 8-bit ADC

$f_{clk} = 100\,KHz$

$$T_{clk} = \frac{1}{100\,KHz}.$$

$$\text{Time to reach } V_{FS} = 2^8 \times T_{clk} = \frac{2^8}{100 \times 10^3} = 2.56\,ms$$

$$\text{Average Conversion time} = \frac{1}{2} \text{ Conversion time}$$

$$= 1.28\,ms.$$

Advantages.

(1) The counter type A/D converter is very simple and needs less hardware compared to the simultaneous-type A/D converter.

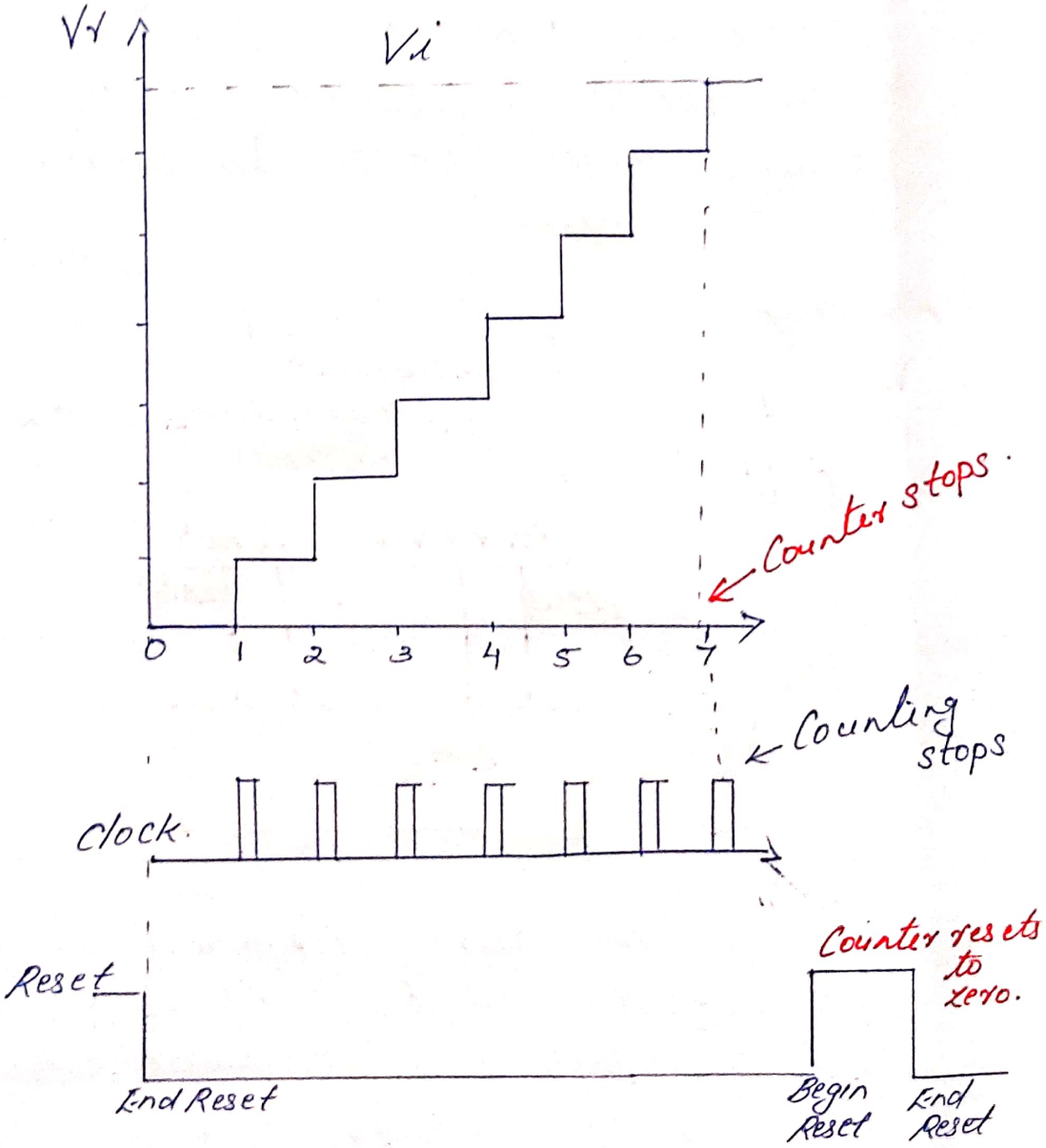
(2) This is suitable for designing applications with high resolution

Disadvantages.

Conversion-time is long & proportional to the amplitude of the analog input voltage.

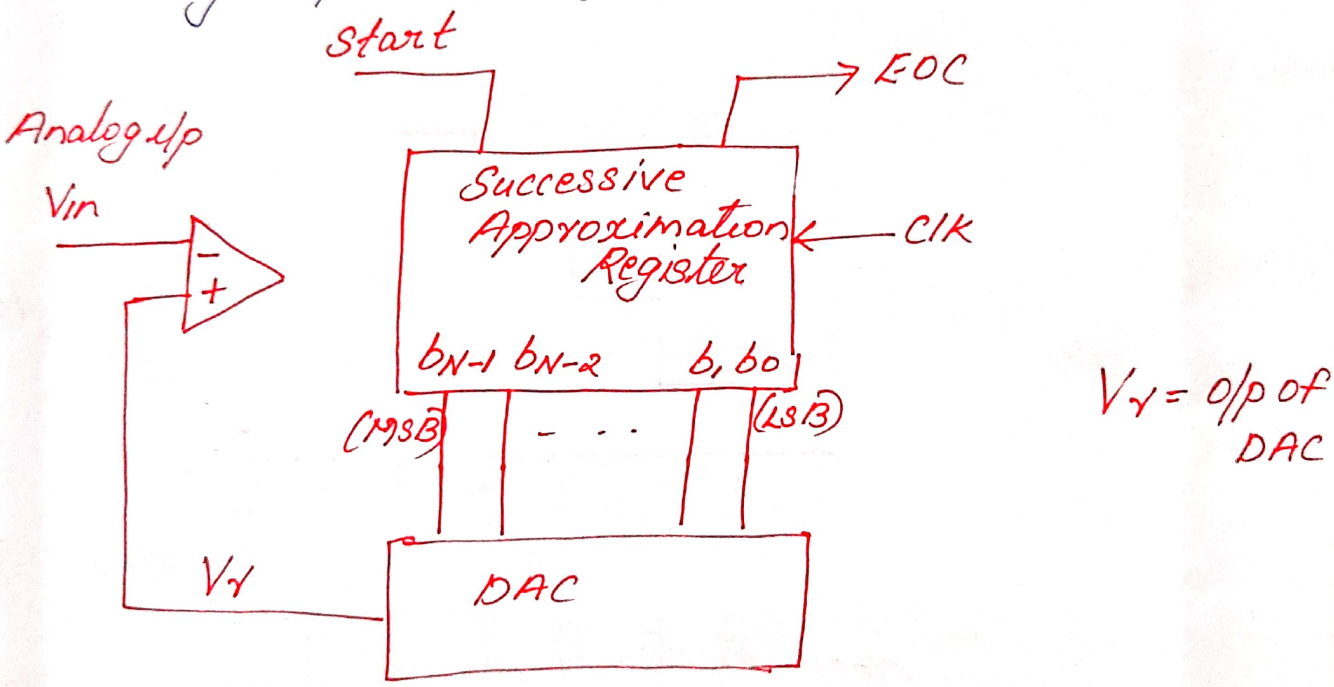
Average Conversion time 2^{n-1} times the clock period

$$\frac{2^N}{2} \times T_{clk}.$$



3. Successive Approximation ADC

The circuit employs a successive approximation register (SAR) which finds the required value of each successive bit by trial and error method. The output of the SAR is fed to an n-bit D/A converter. The analog output equivalent of the D/A converter is applied to the non-inverting input of the comparator. While the other input of the comparator is connected with an unknown analog input voltage Vin under conversion.



When the START command is applied, the SAR sets the MSB(b_{N-1}) of the digital signal, while the other bits are made zero.

Eg:- for a 8-bit ADC, code is 10000000,

The output of the SAR is converted into analog equivalent Vf and gets compared with the input signal Vin.

If V_{in} is greater than the D/A converter output, then the code 10000000 is less than the correct digital value. The MSB is retained as '1' and the next significant bit b_{N-2} is made '1' and the testing is repeated.

by applying clk signal.

Now the code is 11000000.

Its analog equivalent V_r is compared with V_{in}.

If $V_i < V_r$; then the code 1100 0000 is greater than the exact digital equivalent.

∴ the comparator resets the second MSB (b_{N-2}) to zero. and proceeds to b_{N-3}.

This process is repeated for all the remaining bits in the sequence until all the bit positions are tested. The End of Conversion (EOC) signal is sent out when all the bits are tested

Here the D/A converter output voltage gets successively closer to the analog input voltage (V_{in}).

Conversion - time.

It is the sum of ① the time required for reseting SAR before performing the conversion [1 clk] and ② the time required for conversion. [N clks]

$(N+1)T_{clk}$ N = number of bits.

Conversion time is constant & not depends on the analog input voltage.